Dual 5V, 2A Synchronous Step-Down DC/DCs in Tiny LQFN and WLCSP

FEATURES

- **Dual Outputs Each with 2A Output Current**
- **High Efficiency: 19mΩ NMOS and 75mΩ PMOS**
- **Wide Bandwidth, Fast Transient Response**
- **Switching Frequency Synchronizable Up to 3MHz**
- V_{IN} Range: 2.25V to 5.5V
- V_{OUT} Range: 0.5V to V_{IN}
- V_{OUT} Accuracy: ±1%
- Low Ripple Burst Mode® Operation
- Peak Current Mode Control
- Minimum On-Time: 25ns
- Safely Tolerates Inductor Saturation in Overload
- Shutdown Current: 1.2µA
- Precision 400mV Enable Thresholds
- Internal Soft-Start and Compensation
- Power Good Output
- Low Profile, Thermally Enhanced 12-Lead 2mm × 2mm × 0.74mm LQFN and 16-Ball 1.64mm × 1.64mm × 0.5mm WLCSP Packages
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Servers, Telecom Supplies, Optical Networking
- Distributed DC Power Systems (POL)
- FPGA, ASIC, µP Core Supplies
- Industrial/Automotive/Communications

DESCRIPTION

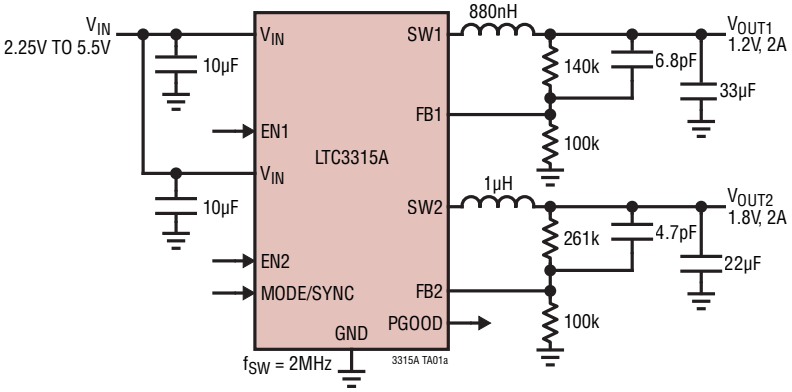
LTC3315AIV features dual 2A monolithic synchronous step-down converters operating from a 2.25V to 5.5V input supply in one package for space-constrained applications with demanding performance requirements. Using constant frequency, peak current mode control at switching frequencies up to 3MHz with a minimum on-time as low as 25ns, both bucks achieve high efficiency and fast transient response in a very small application footprint.

The LTC3315A operates in forced continuous or pulse-skipping mode for low noise or in Burst Mode® operation for high efficiency at light loads. The common buck switching frequency is 2MHz and can be synchronized to an external oscillator via the MODE/SYNC pin.

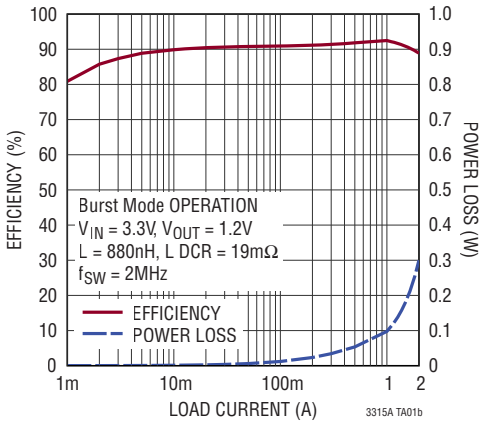
The LTC3315A can regulate outputs as low as 500mV. Other features include precision enable thresholds, a PGOOD signal, output overvoltage protection, thermal shutdown, output short-circuit protection, and up to 100% duty cycle operation for low dropout. The LTC3315A is available in a compact 2mm × 2mm LQFN package and a 1.64mm × 1.64mm WLCSP package.

TYPICAL APPLICATION

Dual 2MHz 2A Buck Regulators



Efficiency vs Load Current



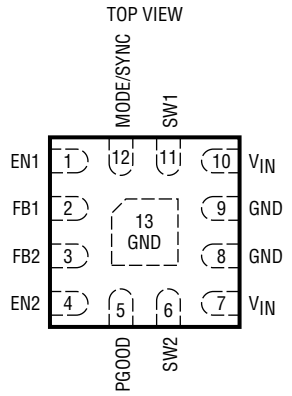
Rev. B

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} ..... –0.3V to 6V
EN1, EN2 ..... –0.3V to Lesser of (V_{IN} + 0.3V) or 6V
FB1, FB2 ..... –0.3V to Lesser of (V_{IN} + 0.3V) or 6V
MODE/SYNC ..... –0.3V to Lesser of (V_{IN} + 0.3V) or 6V
PGOOD ..... –0.3V to 6V
I_{PGOOD} 5mA

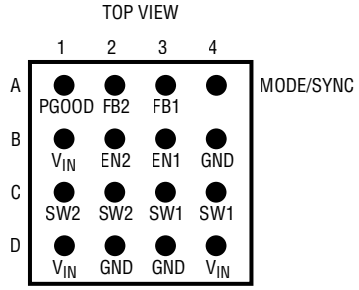
Operating Junction Temperature (Notes 2, 3):
LTC3315AA ..... –40°C to 125°C
LTC3315AE ..... –40°C to 125°C
LTC3315AI ..... –40°C to 125°C
LTC3315AJ ..... –40°C to 150°C
LTC3315AH ..... –40°C to 150°C
LTC3315AMP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Reflow (Package Body) Temperature ... 260°C

PIN CONFIGURATION



LQFN PACKAGE
12-LEAD (2mm × 2mm × 0.74mm)

T_{JMAX} = 150°C, θ_{JA} = 51°C/W, $\theta_{JCBOTTOM}$ = 8.6°C/W,
θ_{JCTOP} = 80°C/W, θ_{JB} = 12°C/W, Ψ_{JT} = 0.8°C/W,
θ AND Ψ VALUES DETERMINED PER JESD51-7 ON A JEDEC 2S2P PC
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB



WLCSP PACKAGE
CB-16-11
16-BALL (1.64mm × 1.64mm × 0.5mm)

T_{JMAX} = 125°C, θ_{JA} = 58°C/W, θ_{JCTOP} = 2.7°C/W,
θ_{JB} = 14.8°C/W, Ψ_{JT} = 2.1°C/W, Ψ_{JB} = 15°C/W
θ AND Ψ VALUES DETERMINED PER JESD51-7 ON A JEDEC 2S2P PC

ORDER INFORMATION

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING* DEVICE	PART MARKING* FINISH CODE	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
LTC3315AEV#TRMPBF	LTC3315AEV#TRPBF	LHFY	e4	LQFN (Laminate Package with QFN Footprint)	MSL 3	–40°C to 125°C
LTC3315AIV#TRMPBF	LTC3315AIV#TRPBF					–40°C to 125°C
LTC3315AJV#TRMPBF	LTC3315AJV#TRPBF					–40°C to 150°C
LTC3315AHV#TRMPBF	LTC3315AHV#TRPBF					–40°C to 150°C
LTC3315AMPV#TRMPBF	LTC3315AMPV#TRPBF					–55°C to 150°C
	LTC3315AACBZ-R7	3315A	e1	WLCSP (16-Ball Wafer Level Chip Scale Package)	MSL1	–40°C to 125°C
AUTOMOTIVE PRODUCTS**						
LTC3315AEV#WTRMPBF	LTC3315AEV#WTRPBF	LHFY	e4	LQFN (Laminate Package with QFN Footprint)	MSL 3	–40°C to 125°C
LTC3315AIV#WTRMPBF	LTC3315AIV#WTRPBF					–40°C to 125°C
LTC3315AJV#WTRMPBF	LTC3315AJV#WTRPBF					–40°C to 150°C
LTC3315AHV#WTRMPBF	LTC3315AHV#WTRPBF					–40°C to 150°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Device temperature grade is indicated by a label on the shipping container.
- TRM = 500 pieces.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings
- Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Notes 2, 3). V_{IN} = 3.3V unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply						
Operating Supply Voltage (V_{IN})		●	2.25		5.5	V
V_{IN} Undervoltage Lockout V_{IN} Undervoltage Lockout Hysteresis	V_{IN} Rising	●	2.05	2.15 150	2.25	V mV
V_{IN} Quiescent Current in Shutdown				1.2	2	µA
V_{IN} Quiescent Current with One Buck Enabled	Burst Mode, Buck in Regulation, Sleeping All Modes, Not Sleeping (Note 4)			45 1.5	70 2.3	µA mA
V_{IN} Quiescent Current with Both Bucks Enabled	Burst Mode, Bucks in Regulation, Sleeping All Modes, Not Sleeping (Note 4)			70 2.8	110 4.2	µA mA
Enable Threshold Enable Threshold Hysteresis	V_{EN} Rising	●	375	400 50	425	mV mV
EN Pin Leakage	V_{EN} = 5.5V				±20	nA
Voltage Regulation, Buck 1 and Buck 2						
Regulated Feedback Voltage (V_{FB})		●	495	500	505	mV
Feedback Voltage Line Regulation	2.25V ≤ V_{IN} ≤ 5.5V			0.015	0.05	%/V
Feedback Pin Input Current	V_{FB} = 500mV				±20	nA
PMOS Current Limit (I_{LIM})	Current out of SW, V_{OUT}/V_{IN} ≤ 0.2		2.9	3.2	3.5	A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Notes 2, 3). V_{IN} = 3.3V unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NMOS Current Limit (I_{VALLEY})	Current out of SW		2.4	2.7	3.0	A
NMOS Reverse Current Limit	Current into SW, Forced Continuous, LQFN		0.5	1	1.5	A
	Current into SW, Forced Continuous, WLCSP		0.5	1	1.7	A
PMOS ON-Resistance				75		mΩ
NMOS ON-Resistance				19		mΩ
SW Leakage Current	Shutdown, V_{IN} = 5.5V				±200	nA
Minimum On Time	V_{IN} = 5.5V	●		25	45	ns
Maximum Duty Cycle		●	100			%
Overtemperature Shutdown (OT) Overtemperature Shutdown Hysteresis	Temperature Rising (Note 5)			165 5		°C °C
Power Good/Soft-Start						
PGOOD Rising Threshold PGOOD Hysteresis	As a Percentage of the Regulated V_{OUT}	● ●	97 0.6	98 1.1	99 1.6	% %
Overvoltage Rising Threshold Overvoltage Hysteresis	As a Percentage of the Regulated V_{OUT}	● ●	107 1	110 2.2	114 3.5	% %
PGOOD Delay				120		µs
PGOOD Leakage Current	V_{PGOOD} = 5.5V				20	nA
PGOOD Pull-Down Resistance	V_{PGOOD} = 0.1V			10	20	Ω
Soft-Start Time	(Note 6)	●	0.25	1	3	ms
Oscillator and MODE/SYNC						
Internal Oscillator Frequency (f_{SW})		●	1.85	2	2.15	MHz
Synchronization Frequency Range		●	1		3	MHz
Minimum SYNC High or Low Pulse Width		●	40			ns
SYNC Level High on MODE/SYNC SYNC Level Low on MODE/SYNC		● ●	1.2		 0.4	V V
MODE/SYNC No Clock Detect Time				10		µs
MODE/SYNC Pin Threshold	For Programming Pulse Skipping Mode For Programming Burst Mode	● ●	 V_{IN} – 0.1		0.1	V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3315A is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3315AE is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LTC3315AI is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3315AJV and the LTC3315AH are guaranteed over the –40°C to 150°C operating junction temperature range, and the LTC3315AMP is guaranteed over the –55°C to 150°C operating junction temperature range. The LTC3315AA specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature (T_J in °C) is calculated from ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance. See High Temperature Considerations section for more details.

Note 3: The LTC3315A includes overtemperature protection which protects the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

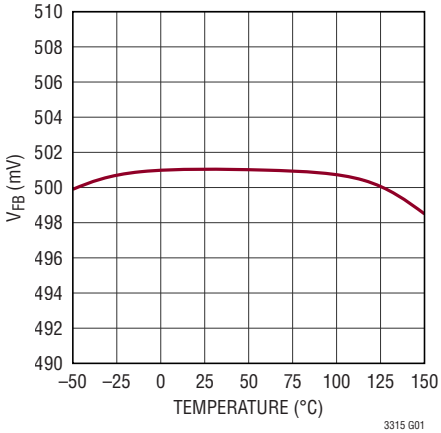
Note 4: Static current, switches not switching. Actual current will be higher due to gate charge losses at the switching frequency.

Note 5: Overtemperature shutdown is not tested in production.

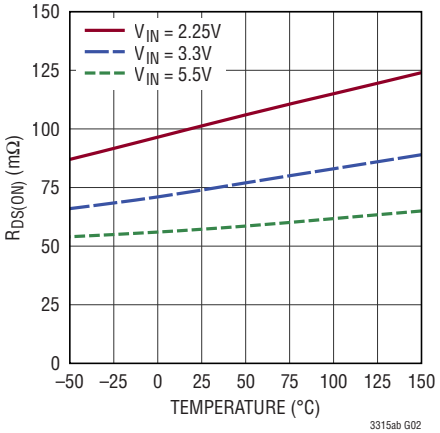
Note 6: The soft-start time is the time from the start of switching until the FB pin reaches 475mV.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{IN} = 3.3V, unless otherwise noted.

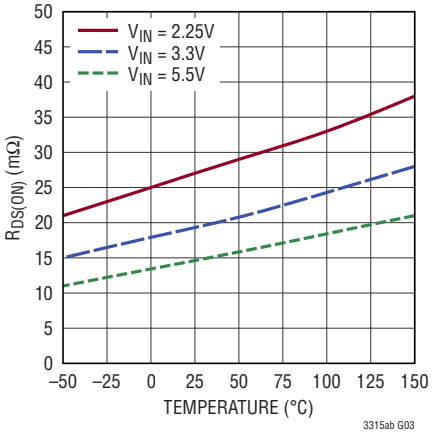
V_{FB} vs Temperature



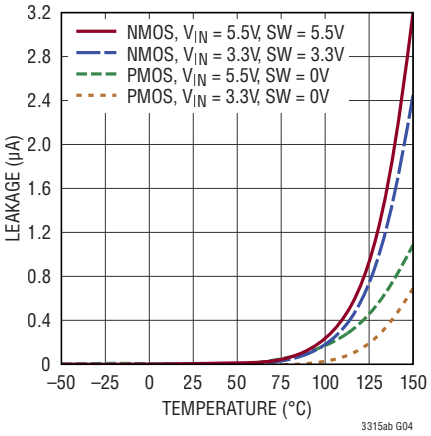
PMOS $R_{DS(ON)}$ vs Temperature



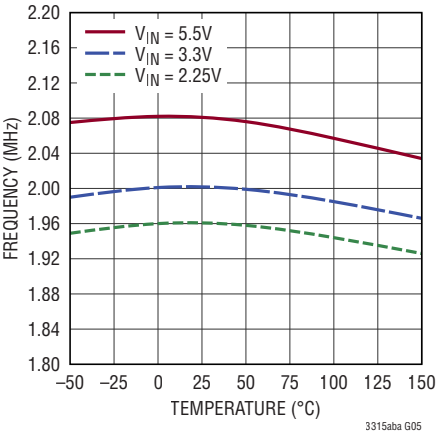
NMOS $R_{DS(ON)}$ vs Temperature



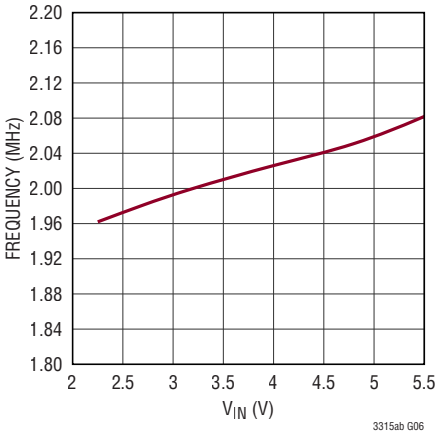
NMOS, PMOS Leakage vs Temperature



Oscillator Frequency vs Temperature



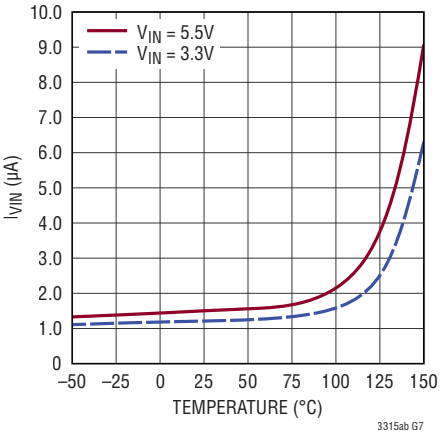
Oscillator Frequency vs V_{IN}



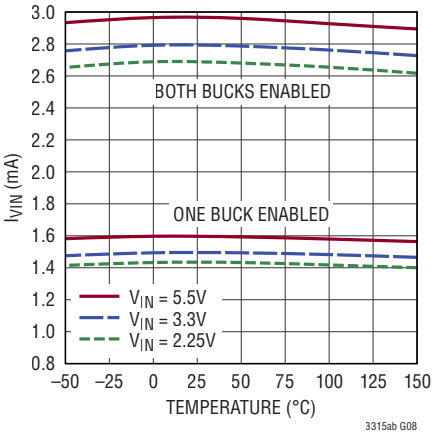
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 3.3V, unless otherwise noted.

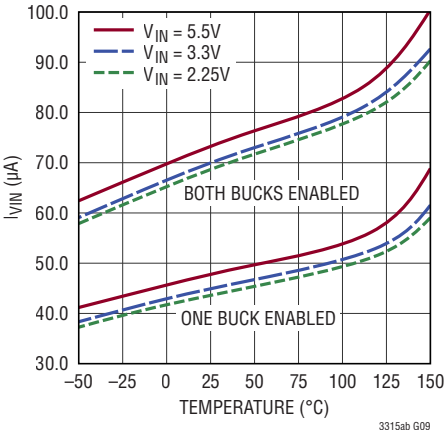
V_{IN} Shutdown Quiescent Current vs Temperature



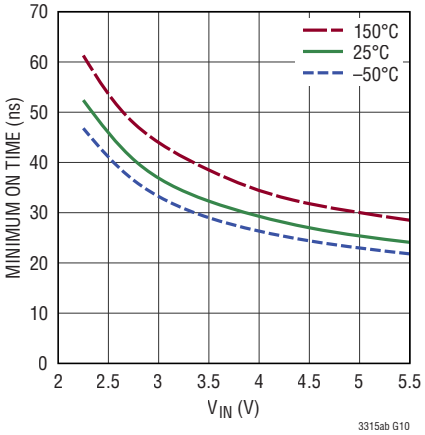
V_{IN} Quiescent Current vs Temperature, All Modes, Not Sleeping



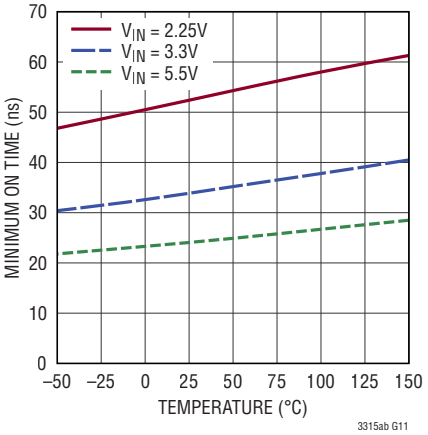
V_{IN} Quiescent Current vs Temperature, Burst Mode, Sleeping



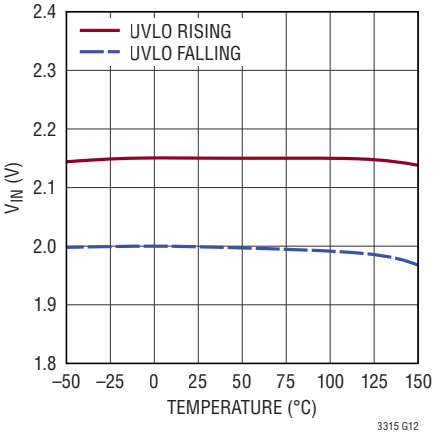
Minimum On Time vs V_{IN}



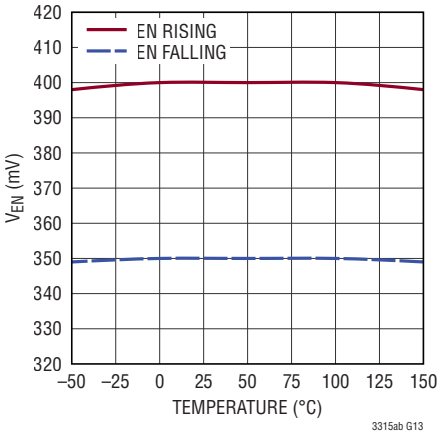
Minimum On Time vs Temperature



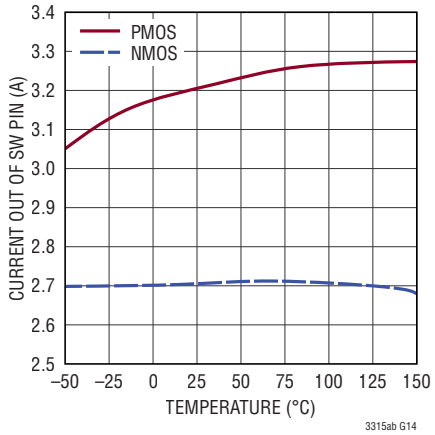
UVLO Threshold vs Temperature



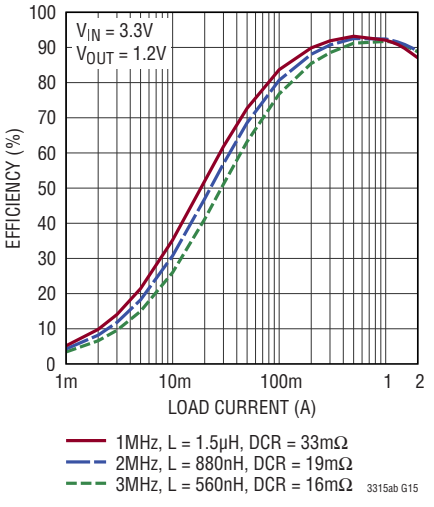
EN Threshold vs Temperature



Current Limit vs Temperature



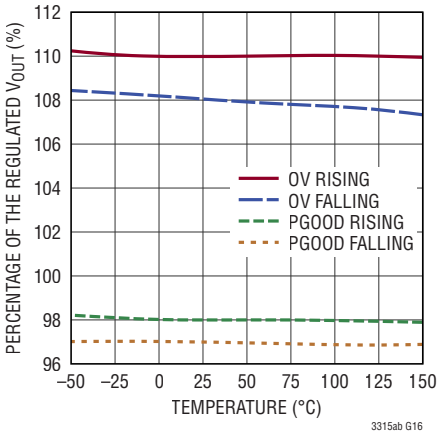
Efficiency vs I_{LOAD} Syncing, Forced Continuous



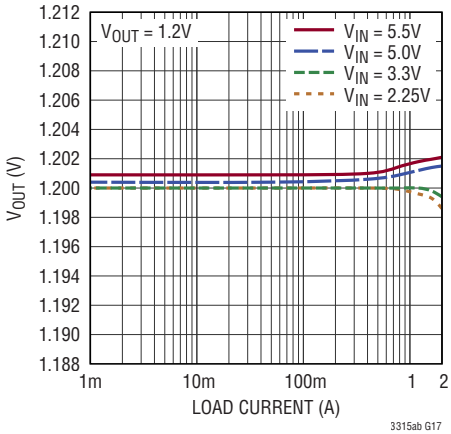
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 3.3V, unless otherwise noted.

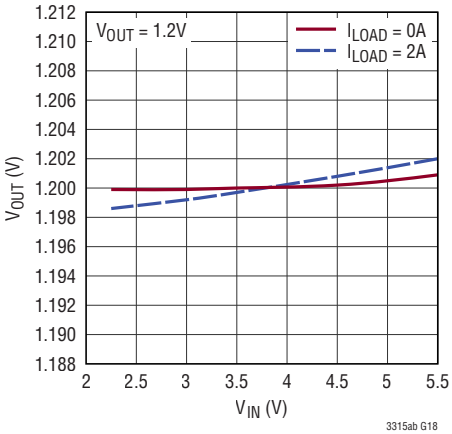
PGOOD, OV vs Temperature



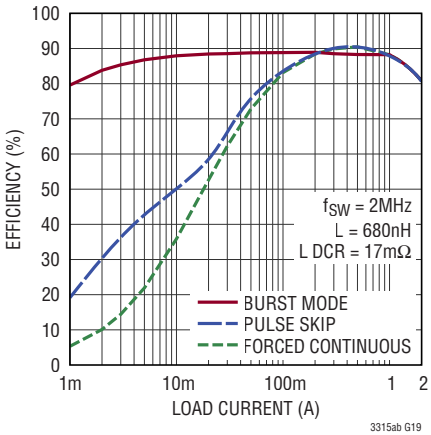
V_{OUT} Load Regulation



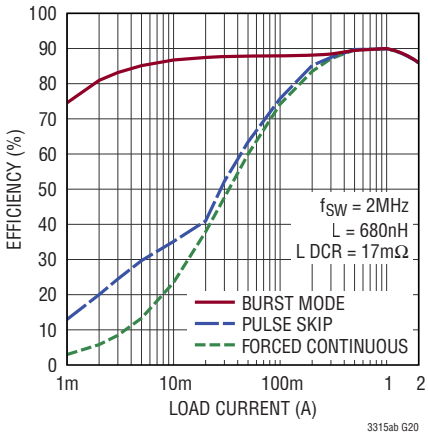
V_{OUT} Line Regulation



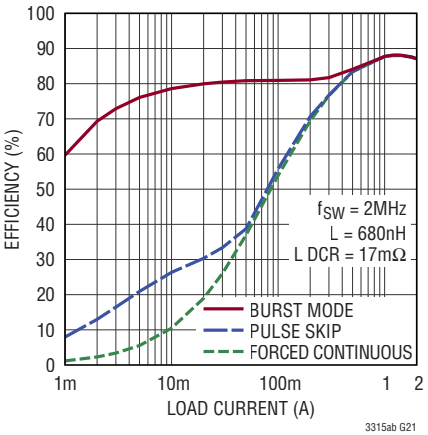
Efficiency vs I_{LOAD}, V_{OUT} = 0.8V, V_{IN} = 2.25V



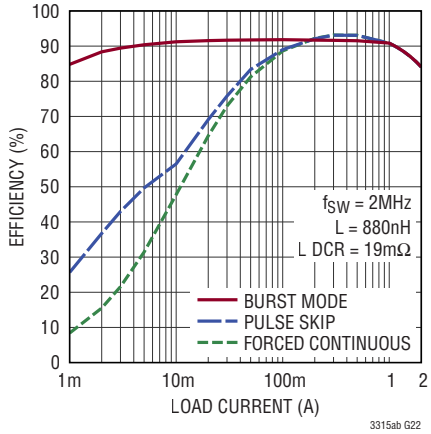
Efficiency vs I_{LOAD}, V_{OUT} = 0.8V, V_{IN} = 3.3V



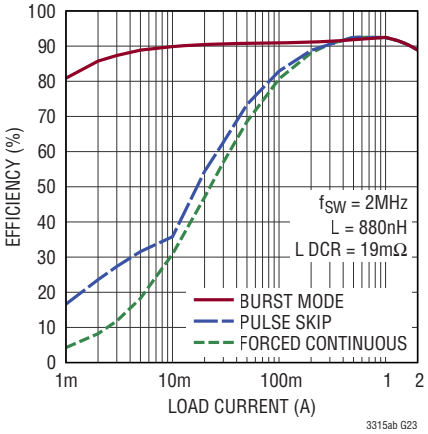
Efficiency vs I_{LOAD}, V_{OUT} = 0.8V, V_{IN} = 5.5V



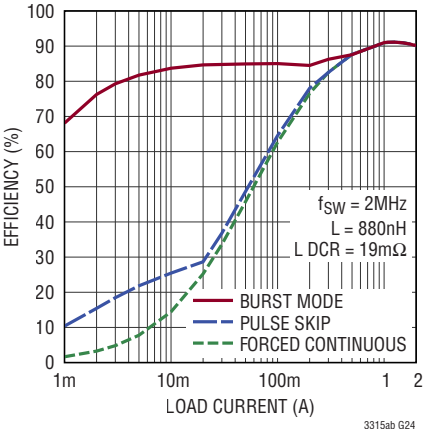
Efficiency vs I_{LOAD}, V_{OUT} = 1.2V, V_{IN} = 2.25V



Efficiency vs I_{LOAD}, V_{OUT} = 1.2V, V_{IN} = 3.3V

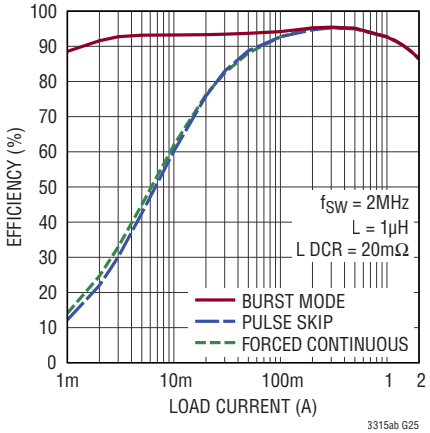


Efficiency vs I_{LOAD}, V_{OUT} = 1.2V, V_{IN} = 5.5V

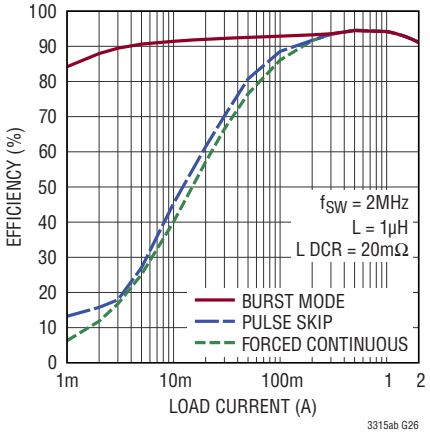


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{IN} = 3.3V, unless otherwise noted.

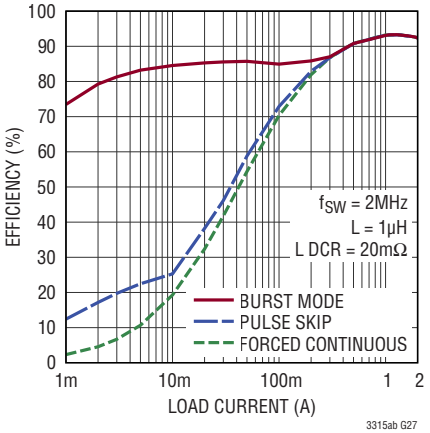
Efficiency vs I_{LOAD}, V_{OUT} = 1.8V, V_{IN} = 2.25V



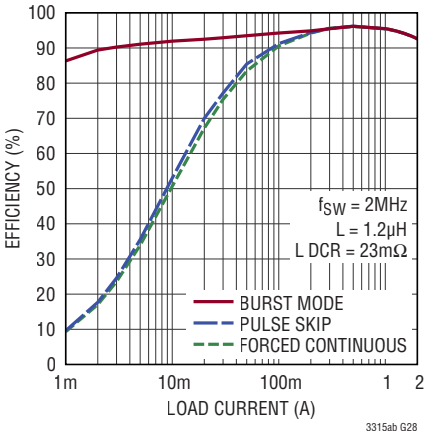
Efficiency vs I_{LOAD}, V_{OUT} = 1.8V, V_{IN} = 3.3V



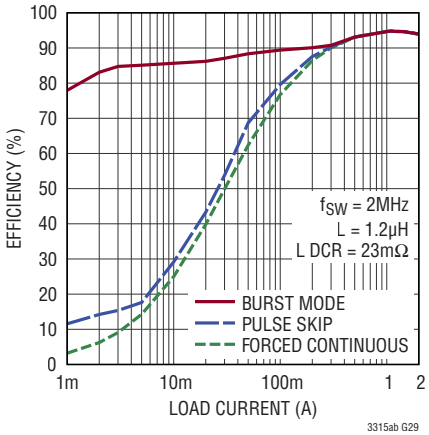
Efficiency vs I_{LOAD}, V_{OUT} = 1.8V, V_{IN} = 5.5V



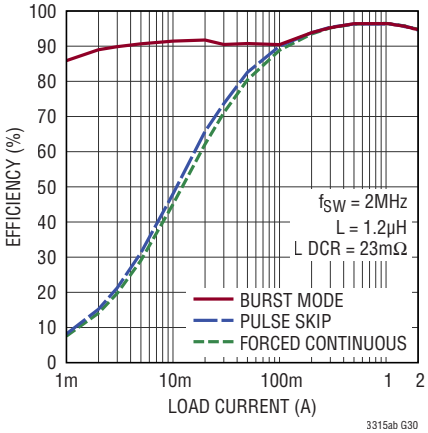
Efficiency vs I_{LOAD}, V_{OUT} = 2.5V, V_{IN} = 3.3V



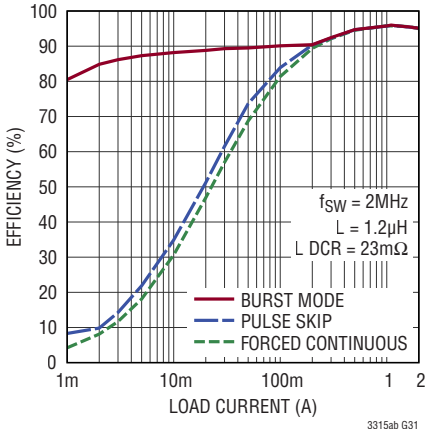
Efficiency vs I_{LOAD}, V_{OUT} = 2.5V, V_{IN} = 5.5V



Efficiency vs I_{LOAD}, V_{OUT} = 3.3V, V_{IN} = 4.2V

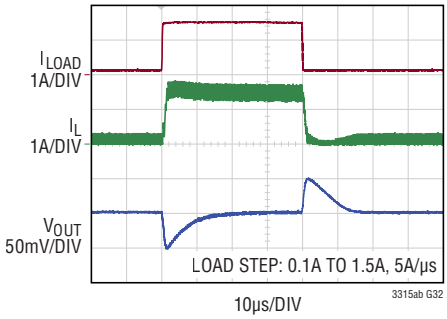


Efficiency vs I_{LOAD}, V_{OUT} = 3.3V, V_{IN} = 5.5V



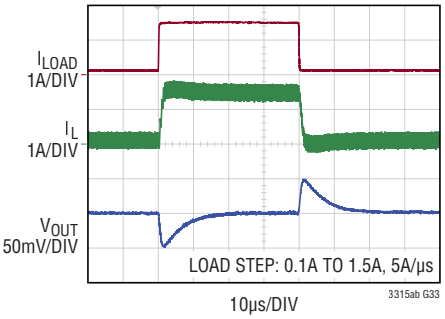
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{IN} = 3.3V, unless otherwise noted.

Transient Response, Pulse Skip Mode



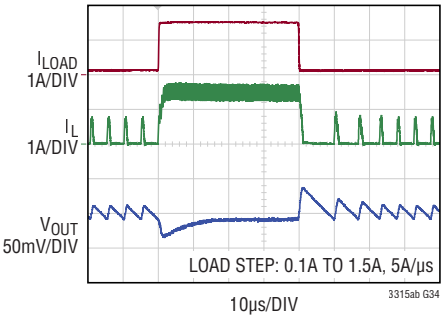
REFER TO BUCK 1 IN TYPICAL APPLICATION: DUAL 1.2V AND 0.8V 2MHz, 2A BUCK REGULATORS, V_{IN} = 3.3V

Transient Response, FC Mode



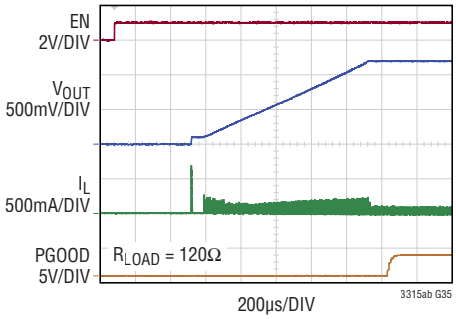
REFER TO BUCK 1 IN TYPICAL APPLICATION: DUAL 1.2V AND 0.8V 2MHz, 2A BUCK REGULATORS, V_{IN} = 3.3V

Transient Response, Burst Mode Operation



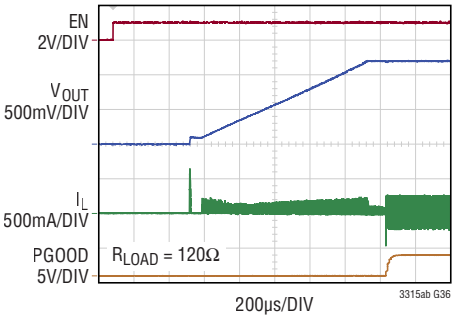
REFER TO BUCK 1 IN TYPICAL APPLICATION: DUAL 1.2V AND 0.8V 2MHz, 2A BUCK REGULATORS, V_{IN} = 3.3V

Startup Transient, Pulse Skip Mode



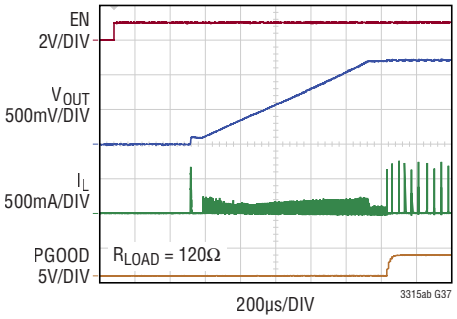
REFER TO BUCK 1 IN TYPICAL APPLICATION: DUAL 1.2V AND 0.8V 2MHz, 2A BUCK REGULATORS, V_{IN} = 3.3V

Startup Transient, FC Mode



REFER TO BUCK 1 IN TYPICAL APPLICATION: DUAL 1.2V AND 0.8V 2MHz, 2A BUCK REGULATORS, V_{IN} = 3.3V

Startup Transient, Burst Mode



REFER TO BUCK 1 IN TYPICAL APPLICATION: DUAL 1.2V AND 0.8V 2MHz, 2A BUCK REGULATORS, V_{IN} = 3.3V

PIN FUNCTIONS (LQFN/WLCSP)

EN1 (Pin 1/Ball B3): Enable Input for Buck Regulator 1. Active high. The EN1 pin has a precision threshold and an optional external resistor divider from V_{IN} or another supply programs when Buck Regulator 1 is enabled. If the precision threshold is not required, drive EN1 to V_{IN} to enable. Do not float.

FB1 (Pin 2/Ball A3): Feedback Input for Buck Regulator 1. Program the output voltage and close the control loop by connecting this pin to the middle node of a resistor divider between the output and ground. The LTC3315A regulates FB1 to 500mV (typical). A phase lead capacitor connected between V_{OUT1} and FB1 may be used to optimize transient response.

FB2 (Pin 3/Ball A2): Feedback Input for Buck Regulator 2. Program the output voltage and close the control loop by connecting this pin to the middle node of a resistor divider between the output and ground. The LTC3315A regulates FB2 to 500mV (typical). A phase lead capacitor connected between V_{OUT2} and FB2 may be used to optimize transient response.

EN2 (Pin 4/Ball B2): Enable Input for Buck Regulator 2. Active high. The EN2 pin has a precision threshold and an optional external resistor divider from V_{IN} or another supply programs when Buck Regulator 2 is enabled. If the precision threshold is not required, drive EN2 to V_{IN} to enable. Do not float.

PGOOD (Pin 5/Ball A1): Power Good Output. Open drain output. When the regulated output voltage of either enabled switching regulator falls below its PGOOD threshold or rises above its overvoltage threshold, this pin is driven low. When both buck regulators are disabled PGOOD is driven low.

SW2 (Pin 6/Balls C1, C2): Switch Node for Buck Regulator 2. Connect an inductor to this pin with a short, wide trace.

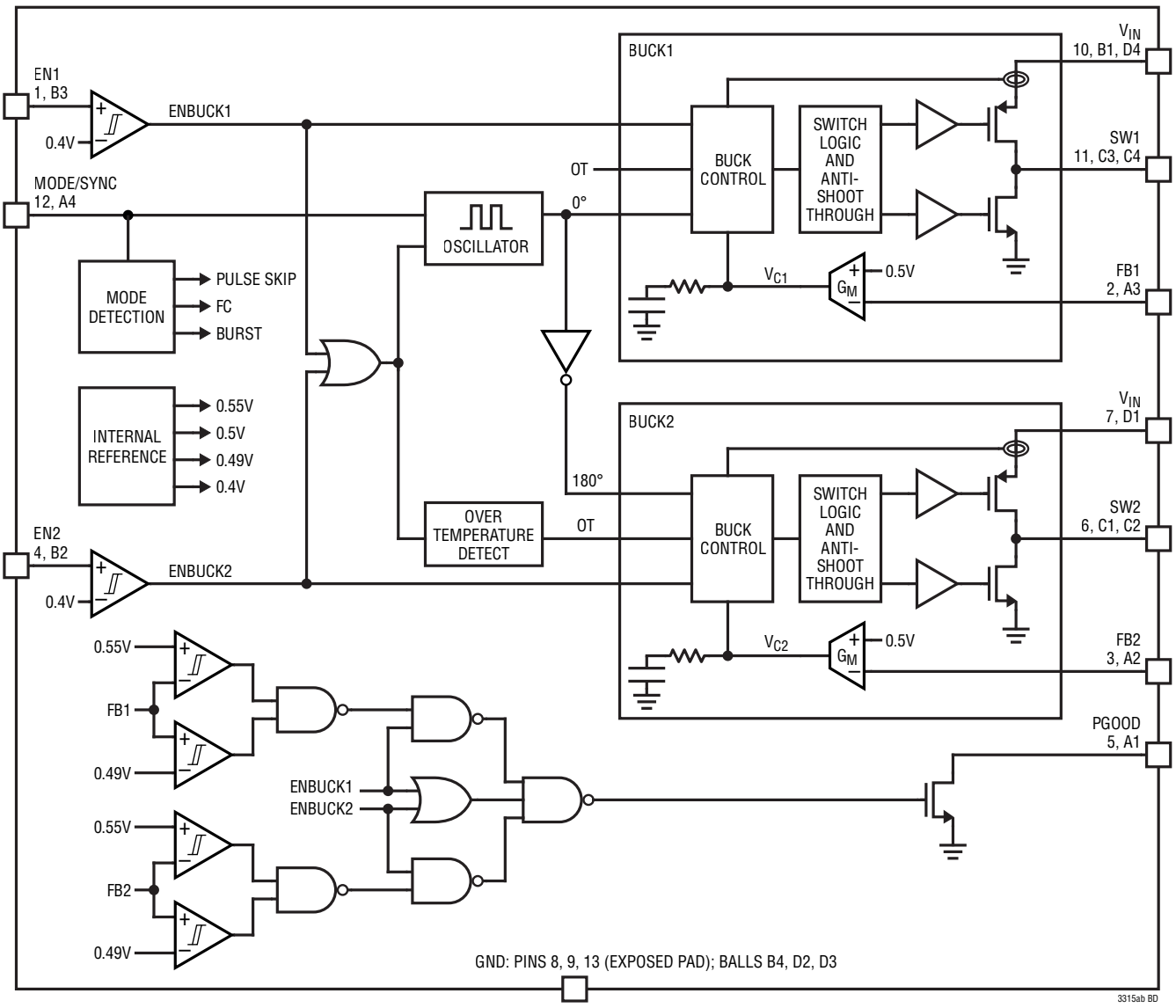
V_{IN} (Pin 7, Pin 10/Balls B1, D1, D4): Input Supply Pins. The V_{IN} pins supply current to internal circuitry and to each buck's PMOS power switch. Connect both V_{IN} pins together with a short, wide trace and bypass to GND with low ESR capacitors located as close as possible to the pins. On the WLCSP package, an optional 0.1µF bypass capacitor can be added to Ball B1 to reduce noise at high V_{IN}.

GND (Pin 8, Pin 9, Exposed Pad Pin 13/Balls B4, D2, D3): Ground. Connect the exposed pad to a continuous ground plane on the printed circuit board directly under the LTC3315A for electrical contact and rated thermal performance. Additionally, Pin 8 and Pin 9 should be shorted to the exposed pad with a wide trace. On the WLCSP package, Balls D2 and D3 can connect on the top of the PCB board to bypass capacitors on V_{IN} and then via to a ground plane on the next layer. Ball B4 can via directly to the ground plane on the next layer.

SW1 (Pin 11/Balls C3, C4): Switch Node for Buck Regulator 1. Connect an inductor to this pin with a short, wide trace.

MODE/SYNC (Pin 12/Ball A4): Mode Selection and External Clock Synchronization Input. Ground this pin to enable pulse-skipping mode. For higher efficiency at light loads, tie this pin to V_{IN} to enable Burst Mode. For fast transient response and constant frequency operation over a wide load range, float this pin to enable forced continuous mode. Drive MODE/SYNC with an external clock to synchronize both buck converters to the applied frequency. When syncing, the operating mode is forced continuous. The slope compensation is automatically adapted to the external clock frequency. In the absence of an external clock both buck converters will switch at the default switching frequency.

BLOCK DIAGRAM



OPERATION

Buck Switching Regulators

The LTC3315A is a 5V dual 2A monolithic, constant frequency, peak current mode step-down DC/DC converter. The synchronous buck switching regulators are internally compensated and require only external feedback resistors to set the output voltage.

An internal oscillator, which can be externally synchronized, turns on the internal PMOS power switch at the beginning of each clock cycle. Current in the inductor ramps up until the PMOS current comparator trips and turns off the PMOS. The peak inductor current, I_{PEAK}, at which the PMOS turns off is controlled by an internal V_C voltage which the error amplifier regulates by comparing the voltage on the feedback (FB) pin with an internal 500mV reference. An increase in the load current causes a reduction in the feedback voltage relative to the reference, causing the error amplifier to raise the V_C voltage (and I_{PEAK}) until the average inductor current matches the new load current. When the PMOS turns off, the NMOS turns on and ramps down the inductor current for the remainder of the clock cycle or, if in pulse skipping mode or Burst Mode, until the inductor current falls to zero. If an overload condition results in excessive current flowing through the NMOS, the next clock cycle will be skipped until the current returns to a safe level.

Each buck switching regulator has its own SW, FB, and EN pins. The buck input supplies are internally connected, but each V_{IN} pin should have its own input bypass capacitor (see Applications Information). The enable pins have precision 400mV thresholds which may be used to provide event-based power-up sequencing by connecting the enable pin to the output of another buck through a resistor divider. If the EN pin of a buck is low, that buck is in shutdown and in a low quiescent current state. If both EN pins are low, both bucks are in shutdown, the SW pins are high impedance, and the quiescent current of the LTC3315A is 1µA (typical). If either EN pin is above the enable threshold of 400mV its respective buck is enabled.

Both buck regulators have forward and reverse inductor current limiting, soft-start to limit inrush current during start-up, and short-circuit protection. When both bucks are disabled and either buck is subsequently enabled, there is a 400µs (typical) delay while internal circuitry powers up followed by a 100µs (typical) no start time before switching commences and the soft-start ramp begins. If a second buck is then enabled, it will also have a 100µs (typical) no start time. If the second buck is enabled within 400µs of the first buck, it will wait until the expiry of the 400µs to begin its no start time.

The buck switching regulators are switched 180° out of phase with respect to each other. The phase determines the fixed edge of the switching sequence, which is when the PMOS turns on. The PMOS off (NMOS on) phase is subject to the regulated duty cycle of each buck.

Mode Selection

The buck switching regulators operate in three different modes set by the MODE/SYNC pin: pulse skipping mode (when the MODE/SYNC pin is set low), forced continuous PWM mode (when the MODE/SYNC pin is floating), and Burst Mode (when the MODE/SYNC pin is set high). The MODE/SYNC pin sets the operating mode for both buck switching regulators.

In pulse skipping mode, the oscillator operates continuously and positive SW transitions are aligned to the clock. Negative inductor current is disallowed and during light loads switch pulses are skipped to regulate the output.

In forced continuous mode, the oscillator runs continuously, no pulses are skipped, and switching occurs in every cycle. To maintain regulation, the inductor current is allowed to reverse under light load conditions. This mode allows the buck to run at a fixed frequency with minimal output ripple. In forced continuous mode if the inductor current reaches –1A (typical, 1A into the SW pin) the NMOS will turn off for the remainder of the cycle to limit the current.

In Burst Mode operation, at light loads, the output capacitor is charged to a voltage slightly higher than its regulation point. The regulator then goes into a sleep state, during which time the output capacitor provides the load current. In sleep most of the regulator's circuitry is powered down, helping to conserve input power. When the output voltage drops below its programmed value, the circuitry is powered back on and another burst cycle begins.

OPERATION

The sleep time decreases as load current increases. In Burst Mode operation, the regulator will burst at light loads whereas at higher loads it will operate in constant frequency PWM mode.

Synchronizing the Oscillator to an External Clock

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values and improves transient response. Operation at lower frequencies improves efficiency by reducing switching losses but requires larger inductance and/or capacitance values to maintain low output voltage ripple. The LTC3315A operates at a default frequency of 2MHz.

The LTC3315A's internal oscillator is synchronized through an internal PLL circuit to an external frequency by applying a square wave clock signal to the MODE/SYNC pin. During synchronization, the Buck 1 PMOS turn-on is locked to the rising edge of the external frequency source. Buck 2 will be 180° out of phase with respect to Buck 1. While syncing, the buck switching regulators operate in forced continuous mode. The synchronization frequency range is 1MHz to 3MHz.

After detecting an external clock on the SYNC pin, the internal PLL starts up at the default frequency. The internal PLL then gradually adjusts its operating frequency to match the frequency and phase of the SYNC signal.

When the external clock is removed the LTC3315A will detect the absence of the external clock within approximately 10µs. During this time it will continue to provide clock cycles. Once the external clock removal has been detected, the oscillator will gradually adjust its operating frequency back to the default.

Power Failure Reporting Via PGOOD Pin

Power failure faults are reported via the PGOOD pin. Both buck switching regulators have an internal power good (PGOOD) signal and if a buck is enabled its internal PGOOD signal must be high for the PGOOD pin to be high. When the regulated output voltage of an enabled buck rises above 98% of its programmed value, the PGOOD signal transitions high. If the regulated output voltage subsequently falls below 97% of its programmed value, the PGOOD signal is pulled low. If either enabled buck's internal PGOOD signal stays low for greater than 120µs, then the PGOOD pin is pulled low, indicating to a microprocessor that a power fault has occurred. The 120µs filter time prevents the pin from being pulled low during a transient event. In addition, whenever PGOOD transitions high there will be a 120µs assertion delay.

The LTC3315A also reports overvoltage conditions at the PGOOD pin. If either enabled buck regulator's output voltage rises above 110% of its programmed value, the PGOOD pin is pulled low after 120µs. Similarly, if all enabled outputs that are overvoltage subsequently fall below 107.8% of their programmed value, the PGOOD pin transitions high again after 120µs.

An error condition that pulls the PGOOD pin low is not latched. When the error condition goes away, the PGOOD pin is released and is pulled high if no other error condition exists. PGOOD is also pulled low in the following scenarios: if neither buck switching regulator is enabled, if V_{IN} is below the UVLO threshold, or if the LTC3315A is over temperature (see below).

Output Overvoltage Protection

During an output overvoltage event, when the FB pin voltage is greater than 110% of its regulated value, the LTC3315A PMOS will be turned off immediately.

An output overvoltage event should not happen under normal operating conditions.

Overtemperature Protection

To prevent thermal damage, the LTC3315A incorporates an overtemperature (OT) function. When the LTC3315A die temperature reaches 165°C (typical, not tested) all enabled buck switching regulators are shut down and remain in shutdown until the die temperature falls to 160°C (typical, not tested).

OPERATION

Output Voltage Soft-Start

Soft starting the output prevents current surge on the input supply and/or output voltage overshoot. During soft-start, the output voltage will proportionally track an internal voltage ramp. An active pull-down circuit discharges that internal voltage in the case of fault conditions. The ramp will restart when the fault is cleared. Fault conditions that initiate the soft-start ramp are the V_{IN} voltage falling too low or thermal shutdown.

Recovery from an output short-circuit (see below) may involve another soft-start cycle if the FB voltage falls more than 120mV (typical) below regulation. During such a recovery, the FB voltage will quickly charge up to 120mV (typical) and then follow the soft-start ramp until regulation is reached.

Dropout Operation

As the input supply voltage approaches the output voltage, the duty cycle increases toward 100%. Further reduction of the supply voltage forces the PMOS to remain on for more than one cycle, eventually reaching 100% duty cycle. The output voltage will then be determined by the input voltage minus the DC voltage drop across the internal PMOS and the inductor.

Low Supply Operation

The LTC3315A is designed to operate down to an input supply voltage of 2.25V. An important thermal design consideration is that the $R_{DS(ON)}$ of the power switches increases at low input. Consider the worst case LTC3315A power dissipation and die junction temperature at the lowest input voltage.

Output Short-Circuit Protection and Recovery

The peak inductor current level at which the current comparator shuts off the PMOS is controlled by the error amplifier. When the output current increases, the error amplifier raises the internal V_C voltage until the average inductor current matches the load current. The LTC3315A clamps the maximum internal V_C voltage, thereby limiting the peak inductor current.

When the output is shorted to ground, the inductor current decays very slowly during the downslope because the voltage across the inductor is low. To keep the inductor current in control a secondary limit is imposed on the valley of the inductor current. If the inductor current measured through the NMOS remains greater than I_{VALLEY} at the end of the cycle, the PMOS will be held off. Subsequent switching cycles will be skipped until the inductor current falls below I_{VALLEY}.

APPLICATIONS INFORMATION

Buck Switching Regulator Output Voltage and Feedback Network

The output voltage of the buck switching regulators is programmed by a resistor divider connected from the switching regulator's output to ground and is given by:

$$V_{OUT} = V_{FB}\left(1+\frac{R2}{R1}\right) \quad (1)$$

as shown in Figure 1 where V_{FB} = 500mV. Typical values for R1 range from 40kΩ to 1MΩ. 1% resistors are recommended to maintain output voltage accuracy. The buck regulator transient response may improve with an optional phase lead capacitor C_{FF} that helps cancel

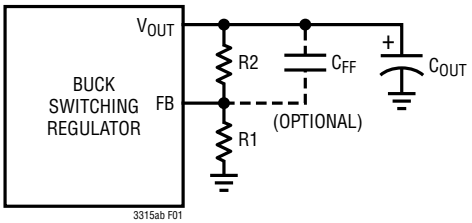


Figure 1. Feedback Components

the pole created by the feedback resistors and the input capacitance of the FB pin. Experimentation with capacitor values between 2pF and 22pF may improve transient response. The values used in the typical application circuits are a good starting point.

APPLICATIONS INFORMATION

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, transient response, and input voltage range. The LTC3315A can operate at frequencies between 1MHz and 3MHz.

The advantage of high frequency operation is that smaller inductor and capacitor values may be used. Higher switching frequencies allow for higher control loop bandwidth and, therefore, faster transient response. The disadvantages of higher switching frequencies are lower efficiency, because of increased switching losses, and a smaller input voltage range, because of minimum switch on-time limitations.

The minimum on-time of the buck regulator imposes a minimum operating duty cycle. The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT}}{t_{ON(MIN)} \bullet V_{IN(MAX)}} \quad (2)$$

where $V_{IN(MAX)}$ is the maximum input voltage, V_{OUT} is the output voltage and $t_{ON(MIN)}$ is the minimum top switch on-time. This equation shows that a slower switching frequency might be necessary to accommodate a high V_{IN}/V_{OUT} ratio.

The LTC3315A is capable of a maximum duty cycle of 100%, therefore, the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the PMOS, the inductor DCR, and the load current.

Inductor Selection and Maximum Output Current

Considerations in choosing an inductor are inductance, RMS current rating, saturation current rating, DCR, and core loss.

Select the inductor value based on the following equations:

$$L \approx \frac{V_{OUT}}{0.6A \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} \leq 0.5 \quad (3)$$

$$L \approx \frac{V_{IN(MAX)}}{2.4A \bullet f_{SW}} \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} > 0.5 \quad (4)$$

where f_{SW} is the switching frequency and $V_{IN(MAX)}$ is the maximum applied input voltage.

To avoid overheating of the inductor, choose an inductor with an RMS current rating that is greater than the maximum expected output load of the application. Overload and short-circuit conditions need to be taken into consideration.

In addition ensure that the saturation current rating (typically labeled I_{SAT}) is either higher than 3.5A, the maximum current limit of the LTC3315A, or higher than the maximum expected load plus half the inductor ripple:

$$I_{SAT} > I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (5)$$

where $I_{LOAD(MAX)}$ is the maximum output load current for the application and ΔI_L is the inductor ripple current calculated as:

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

To keep the efficiency high, choose an inductor with the lowest series resistance (DCR) and a core material intended for high frequency applications. Table 1 shows recommended inductors from several manufacturers.

Input Capacitors

Bypass the input of the LTC3315A with at least two ceramic capacitors, one near each V_{IN} pin for best performance. Connect the ground of each capacitor to a wide PCB trace on the top layer of the PCB that connects pins 8 and 9 with the exposed pad. These capacitors should be 0603 or 0805 in size. Smaller 0201 capacitors can also be placed as close as possible to the LTC3315A directly on the traces leading from V_{IN} (Pin 7) and GND (Pin 8) and on the traces leading from V_{IN} (Pin 10) and GND (Pin 9) to reduce input noise with minimal (if at all) increase in application footprint. See the layout section for more detail. On the WLCSP package, an optional 0.1µF bypass capacitor can be added to Ball B1 to reduce noise at high V_{IN}. X7R or X5R capacitors are recommended for best performance across temperature and input voltage variations (see Table 2). Note that larger input capacitance is

APPLICATIONS INFORMATION

Table 1. Recommended Inductors

MANUFACTURER	FAMILY	L (nH)	MAX IDC (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)
Murata	DFE18SAN_G0	240 - 470	3.6 - 4.9	30 - 54	1.6 × 0.8 × 1.0
Murata	DFE252010F	330 - 680	3.5 - 4.8	21 - 37	2.5 × 2.0 × 1.0
Vishay	IHLP-1212BZ-11	220 - 1500	4.0 - 7.5	11.4 - 32	3.0 × 3.0 × 2.0
Vishay	IHHP-0806AB-01	220 - 470	3.6 - 5.0	16 - 35	2.0 × 1.6 × 1.2
Wurth Elektronik	WE-MAPI	330 - 1500	3.7 - 5.5	17 - 39	3.0 × 3.0 × 2.0
Wurth Elektronik	WE-PMCI	250 - 470	3.6 - 4	12.5 - 31	3.2 × 2.5 × 1.2
Coilcraft	XEL3515	72 - 560	3.2 - 23.7	6.5 - 16	3.5 × 3.2 × 1.5

required when a lower switching frequency is used. If the input power source has high impedance, or if there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with an electrolytic capacitor. A ceramic input capacitor combined with trace or cable inductance forms a high quality (underdamped) tank circuit. If the LTC3315A circuit is plugged in to a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the voltage rating. This situation is easily avoided (see Analog Devices Application Note 88).

Table 2. Ceramic Capacitor Manufacturers

MANUFACTURER	URL
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.tdk.com
Taiyo Yuden	www.t-yuden.com
Samsung	www.samsungsem.com
Wurth Elektronik	www.we-online.com

Output Capacitor, Output Ripple, and Loop Response

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LTC3315A at the SW pin to produce the DC output. In this role it determines the output ripple; thus, low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and to stabilize the LTC3315A's control loop.

The LTC3315A is internally compensated and designed to operate at a high bandwidth for fast transient response capability. The selection of C_{OUT} affects the bandwidth of the system, but the transient response is also affected by V_{OUT}, V_{IN}, f_{SW} and other factors. A good place to start is with an output capacitance value of approximately:

$$C_{OUT} = \frac{80\mu F \bullet MHz}{f_{SW}} \sqrt{\frac{500mV}{V_{OUT}}} \quad (7)$$

where C_{OUT} is the recommended output capacitor value and f_{SW} is the switching frequency. A lower value of output capacitor saves space and cost, but transient performance will suffer and loop stability must be verified. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best output ripple and transient performance. Use X5R or X7R ceramic capacitors. (see Table 2). Even better output ripple and transient performance can be achieved by using low-ESL reverse geometry or three terminal ceramic capacitors.

During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop increases the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. Although affected by V_{OUT}, V_{IN}, f_{SW}, $t_{ON(MIN)}$, the equivalent series inductance (ESL) of the output capacitor, and other factors, the output droop, V_{DROOP}, is usually about 3 times the linear drop of the first cycle:

$$V_{DROOP} = \frac{3 \bullet \Delta I_{OUT}}{C_{OUT} \bullet f_{SW}} \quad (8)$$

where ΔI_{OUT} is the load step.

APPLICATIONS INFORMATION

Transient performance and control loop stability can be improved with a higher C_{OUT} and/or the addition of a feedforward capacitor, C_{FF}, placed between V_{OUT} and FB. Capacitor C_{FF} provides phase lead compensation by creating a high frequency zero which improves the phase margin and the high-frequency response. The values used in the typical application circuits are a good starting point. LTpowerCAD® is a useful tool to help optimize C_{FF} and C_{OUT} for the desired transient performance.

Applying a load transient and monitoring the response of the system or using a network analyzer to measure the actual loop response are two ways to experimentally verify transient performance and control loop stability, and to optimize C_{FF} and C_{OUT}.

When using the load transient response method to stabilize the control loop, apply an output current pulse going from 20% to 100% of full load current having a very fast rise time. This will produce a transient on the output voltage. Monitor V_{OUT} for overshoot or ringing that might indicate a stability problem (see Application Note 149).

Using the Precision Enable Threshold

The LTC3315A has precision threshold enable pins for each buck regulator to enable or disable each buck. When both are forced low, the device enters into a low current shutdown mode.

The rising threshold of both EN comparators is 400mV, with 50mV of hysteresis. The EN pins can be tied to V_{IN} if the shutdown feature is not used. Adding a resistor divider from V_{IN} to an EN pin to ground programs the LTC3315A to regulate that output only when V_{IN} is above a desired voltage.

Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws near constant power from its input source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where problems may occur. Referring to Figure 2, this threshold can

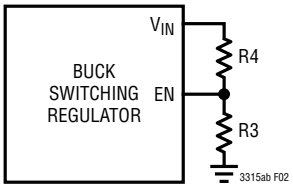


Figure 2. EN Divider

be adjusted by setting the values of R3 and R4 such that they satisfy the following equation:

$$V_{IN(EN)} = 400mV \bullet \left(1 + \frac{R4}{R3}\right) \quad (9)$$

The buck regulator will remain off until V_{IN} is above $V_{IN(EN)}$. The buck regulator will remain enabled until V_{IN} falls to 0.875 • $V_{IN(EN)}$ and EN is 350mV.

Alternatively a resistor divider from the output of one buck to the EN pin of the second buck to ground provides event based power-up sequencing as the first buck reaching regulation enables the second buck. Replace $V_{IN(EN)}$ in Equation 9 with the desired output voltage of the first buck (e.g. 90% of the regulated value) at which the second buck is enabled.

PCB Considerations

The LTC3315A is a high performance IC designed for high efficiency and fast transient response. For optimal results carefully consider the layout of the PCB board and follow the below list to ensure proper operation. Reference the layout design files for the demo board for both the LQFN and WLCSP packages on the LTC3315A product page on the ADI website to see the optimal PCB layout. See Figure 3 for a recommended PCB layout.

1. Connect the exposed pad of the LQFN package (Pin 13) directly to a large, unbroken ground plane under the application circuit on the layer closest to the surface layer to minimize thermal and electrical impedance. Additionally, short the exposed pad to ground pins 8 and 9 on the top layer. See the Application Note, Application Notes for Thermally Enhanced Leaded Plastic Packages document for the proper size and layout of the thermal vias and solder stencils. On the WLCSP package, Balls D2 and D3 can connect on the

APPLICATIONS INFORMATION

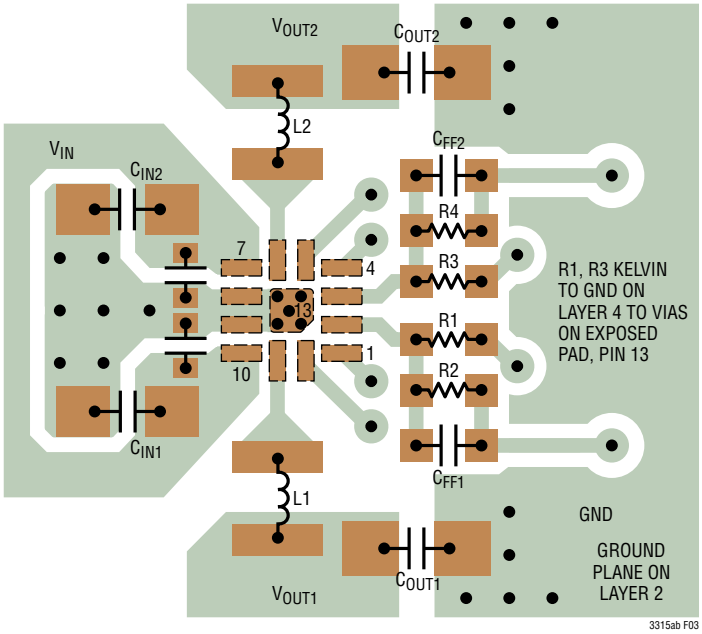


Figure 3. Recommended LTC3315A LQFN PCB Layout

top of the PCB board to bypass capacitors on V_{IN} and then via to a ground plane on the next layer. Ball B4 can via directly to the ground plane on the next layer.

2. Both of the input supply pins should have local decoupling capacitors with their grounded pins connecting on the top layer to the ground plane around pin 8, pin 9, and the exposed pad. These capacitors provide the AC current to the internal power MOSFETs and their drivers. Large, switched currents flow in these capacitors and it is important to minimize inductance from these capacitors by choosing a small case size such as 0603 and placing them close to the V_{IN} pins of the LTC3315A. To further minimize inductance and input noise, smaller 0201 capacitors can be placed as close as possible to the LTC3315A directly on the traces leading from V_{IN} (Pin 7) and GND (Pin 8) and on the traces leading from V_{IN} (Pin 10) and GND (Pin 9) minimal (if at all) increase in application footprint. On the WLCSP package, an optional 0.1µF bypass capacitor can be added to Ball B1 to reduce noise at high V_{IN}.
3. The switching power traces connecting SW1 and SW2 to their respective inductors should be minimized to reduce radiated EMI and parasitic coupling. Due to the large voltage swing on the switching nodes, high input impedance sensitive nodes, such as the feedback nodes, should be kept far away or shielded from the switching nodes or poor performance could result.
4. The GND side of the switching regulator output capacitors connects directly to the thermal ground plane of the IC. Minimize the trace length from the output capacitor to the inductor(s)/pin(s).

High Temperature Considerations

A thermal representation of the LTC3315A thermally enhanced LQFN package is shown in Figure 4 with the silicon die and thermal metrics identified. The current source represents power loss P_D on the die; node voltages represent temperatures; electrical impedances represent conductive thermal impedances $\theta_{JCBOTTOM}$, θ_{JCTOP}, θ_{VIA}, θ_{CB}, and convective thermal impedances θ_{CA} and θ_{BA}. The junction temperature, T_J, is calculated from the ambient temperature, T_A, as:

$$T_J = T_A + P_D \bullet \theta_{JA} \quad (10)$$

where, neglecting the $\theta_{JCTOP} + \theta_{CA}$ path:

$$\theta_{JA} \approx \theta_{JCB} + \left(\frac{\theta_{CB}+\theta_{BA}}{2}\right) \| \left(\frac{\theta_{CB}+\theta_{BA}}{2}+\theta_{VIA}\right) \quad (11)$$

APPLICATIONS INFORMATION

where $\theta_{JCB} = \theta_{JCBOTTOM}$ = 10°C/W. The value of θ_{JA} = 51°C/W reported in the Pin Configuration section corresponds to JEDEC standard 2S2P test PCB, which does not have good thermal vias, i.e., θ_{VIA} is relatively high. Assuming, somewhat arbitrarily but not unreasonably, that $\theta_{VIA} \sim (\theta_{CB} + \theta_{BA})/2$, and back calculating it is seen that $(\theta_{CB} + \theta_{BA})/2 = \theta_{VIA} \approx 60$°C/W for such a board. The importance of thermal vias becomes clear observing that if the test PCB had low-thermal-resistance vias, the θ_{JA} would have been reduced by up to 10°C/W, which is an improvement of up to 20%. Similarly, having more ground planes that are larger, uninterrupted and higher-copper-weight improves $\theta_{CB} + \theta_{BA}$, which has a dominant effect on θ_{JA}, given the low value of $\theta_{JCBOTTOM}$ of the package. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LTC3315A is estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss.

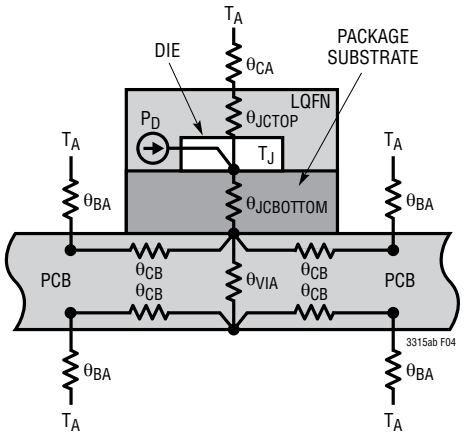
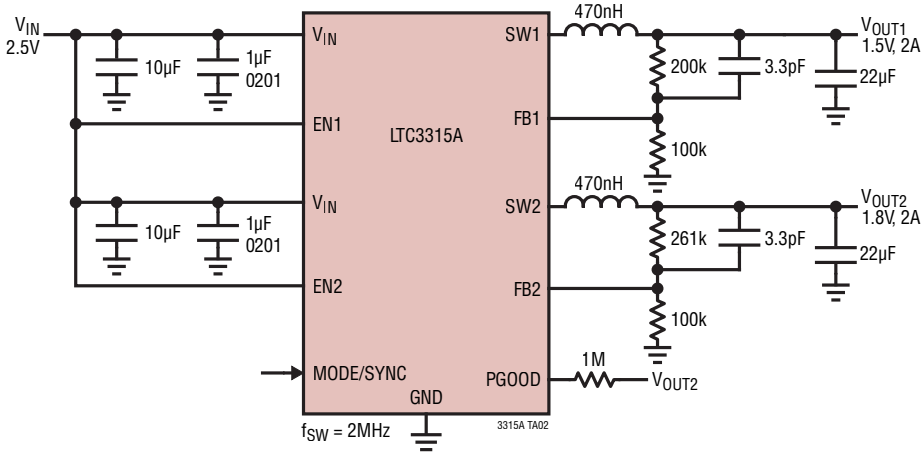


Figure 4. Multi-Layer PCB with Thermal Vias Acts as a Heat Sink

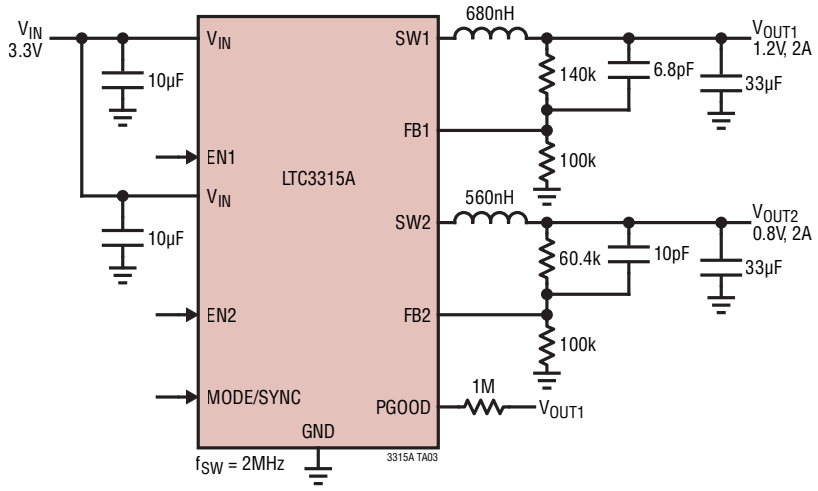
TYPICAL APPLICATIONS

Dual 1.5V and 1.8V 2MHz, 2A Buck Regulators, V_{IN} = 2.5V

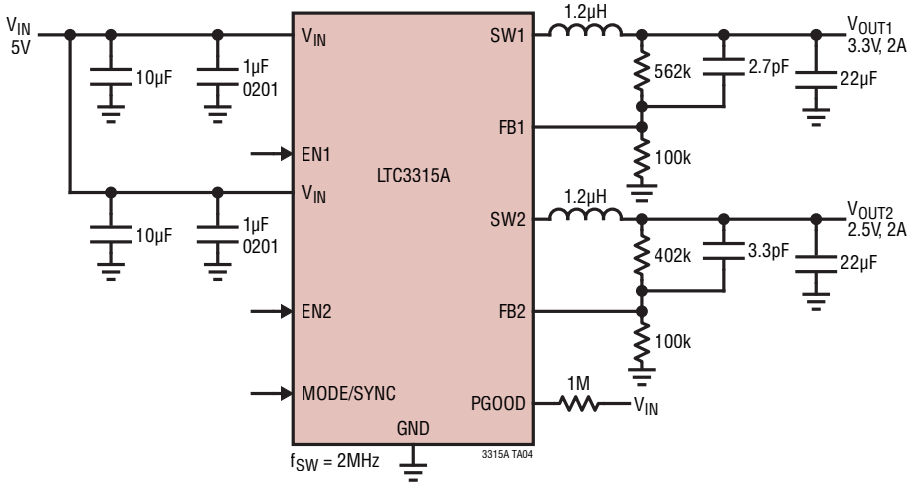


TYPICAL APPLICATIONS

Dual 1.2V and 0.8V 2MHz, 2A Buck Regulators, V_{IN} = 3.3V

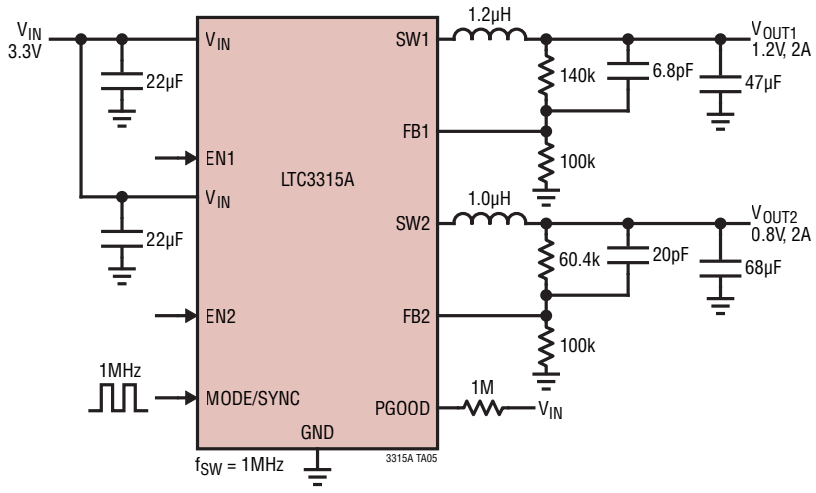


Dual 3.3V and 2.5V 2MHz, 2A Buck Regulators, V_{IN} = 5V

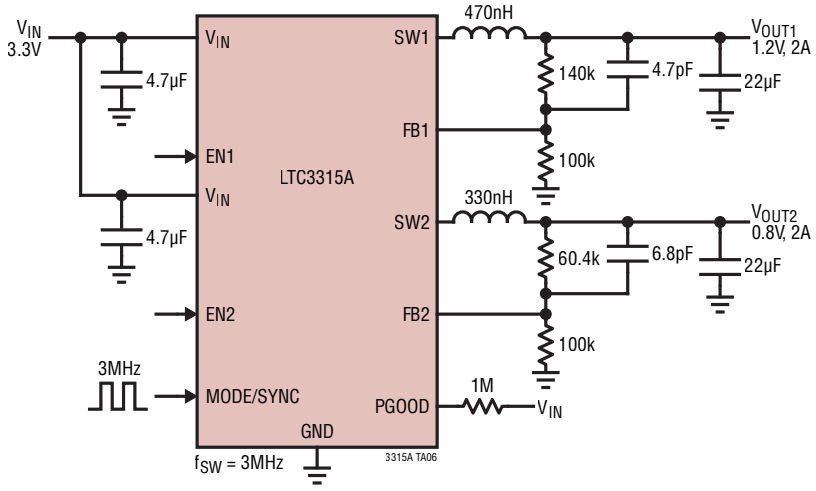


TYPICAL APPLICATIONS

Dual 1.2V and 0.8V 1MHz, 2A Buck Regulators, V_{IN} = 3.3V

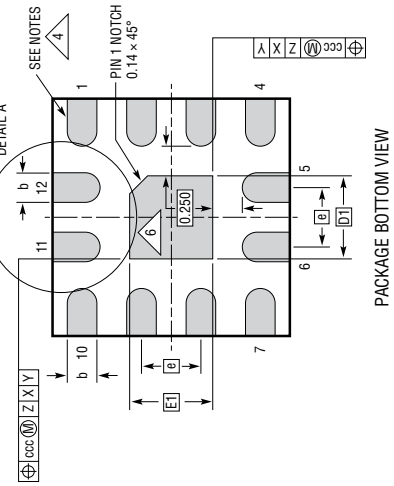


Dual 1.2V and 0.8V 3MHz, 2A Buck Regulators, V_{IN} = 3.3V

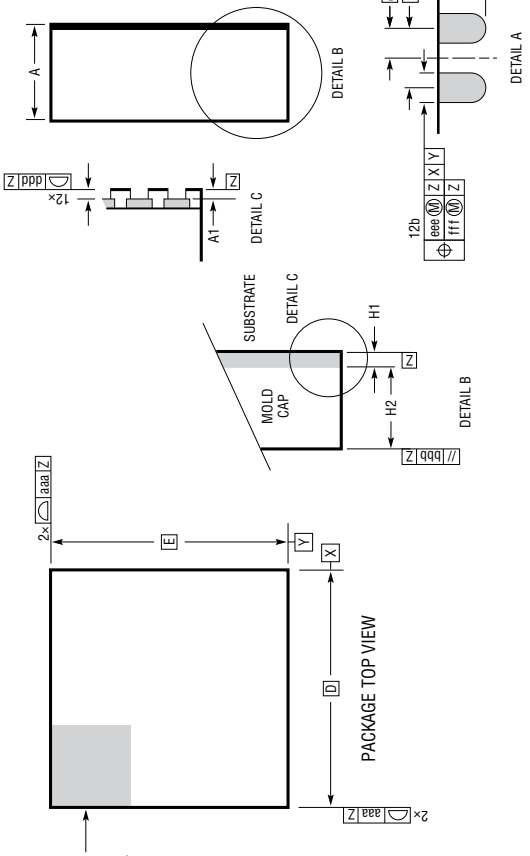


PACKAGE DESCRIPTION

LQFN Package
12-Lead (2mm × 2mm × 0.74mm)
(Reference LTC DWG # 05-08-1530 Rev B)

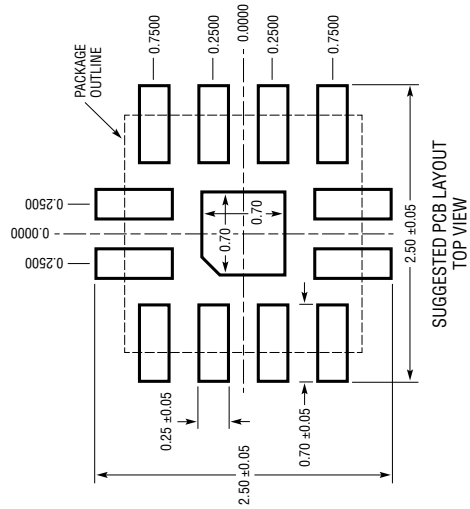


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII



DIMENSIONS

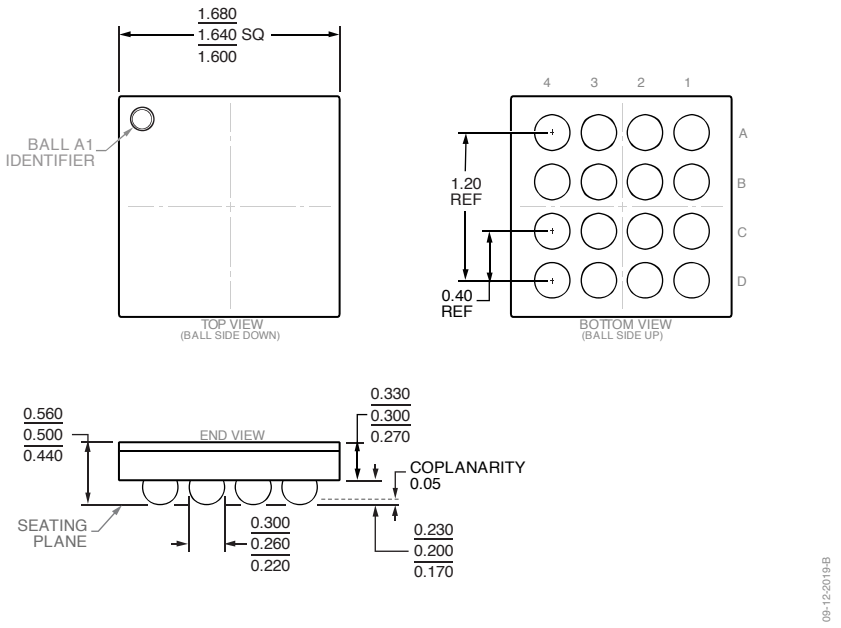
SYMBOL	MIN	NOM	MAX	NOTES
A	0.65	0.74	0.83	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		2.00		
E		2.00		
D1		0.70		
E1		0.70		
e		0.50		
H1		0.24 REF		SUBSTRATE THK
H2		0.50 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	



LQFN 12 0618 REV B

PACKAGE DESCRIPTION

WLCSP PACKAGE
CB-16-11
16-BALL (1.64mm × 1.64mm × 0.5mm)
Dimensions shown in millimeters

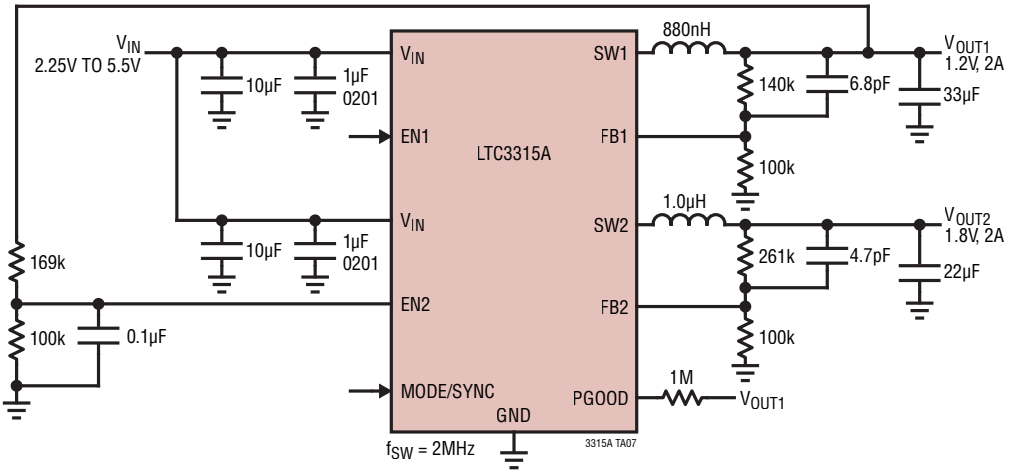


REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/19	Added AEC-Q100 Qualified.	1
		Added #W Flow Part Numbers.	2
B	09/21	Added WLCSP package and references.	1-24
		Revised NMOS Reverse Current Limit spec.	3

TYPICAL APPLICATION

Dual Buck Regulators with Supply Sequencing



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3307A/B, LTC3308A/B, LTC3309A/B	3A, 4A and 6A 5V Synchronous Step-Down Silent Switcher DC/DC in 2mm × 2mm LQFN-12	Monolithic Synchronous Step-Down DC/DC Capable of Supplying up to 6A at Switching Frequencies Up to 3MHz(A) and 10MHz(B). Silent Switcher Architecture for Ultralow EMI Emissions. 2.25V to 5.5V Input Operating Range. 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy. PGOOD Indication, RT Programming, SYNC Input. 2mm × 2mm LQFN-12
LTC3310/ LTC3310S	5V, 10A Synchronous Step-Down Silent Switcher/Silent Switcher 2 in 3mm × 3mm LQFN	Switching Frequencies Up to 5MHz. Silent Switcher/Silent Switcher 2 Architecture for Ultralow EMI Emissions. 2.25V to 5.5V Input Operating Range. 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy. PGOOD Indication, R_T Programming, SYNC Input. Configurable for Paralleling Power Stages. 150°C Operation (LTC3310). Pin Compatible with LTC3311/LTC3311S. 3mm × 3mm LQFN-18 Package.
LTC3370/ LTC3371	4-Channel 8A Configurable 1A Buck DC/DCs	Four Synchronous Buck Regulators with 8 × 1A Power Stages. Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Maximum) with a Single Inductor. 8 Output Configurations Possible. Precision PGOOD Indication. LTC3371 Has a Watchdog Timer. LTC3370: 32-Lead 5mm × 5mm QFN. LTC3371: 38-Lead 5mm × 7mm QFN and TSSOP
LTC3374/ LTC3374A	8-Channel Parallelable 1A Buck DC/DCs	Eight 1A Synchronous Buck Regulators. Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Maximum) with a Single Inductor. 15 Output Configurations Possible. Precision Enable Inputs and PGOOD_ALL Reporting. 38-Lead 5mm × 7mm QFN and TSSOP
LTC3375	8-Channel Parallelable 1A Buck DC/DCs	Eight 1A Synchronous Buck Regulators. Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Maximum) with a Single Inductor. 15 Output Configurations Possible. Precision Enable Inputs and PGOOD_ALL Reporting. I^2C Programming with a Watchdog Timer and Pushbutton. 48-Lead 7mm × 7mm QFN
LT8614	42V, 4A Synchronous Step-Down Silent Switcher® with 2.5µA Quiescent Current	Synchronous Micropower Step-Down DC/DC Converter with Silent Switcher Architecture. Up to 96% Efficiency at 1MHz, $12V_{IN}$ to $5V_{OUT}$. Up to 94% Efficiency at 2MHz, $12V_{IN}$ to $5V_{OUT}$. V_{IN}: 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} <1µA, 18-Lead 3mm × 4mm QFN