Dual Multitopology DC/DC Converters with 2A Switches and Synchronization

FEATURES

- **Dual 2A and One 500mA, 50V Internal Power Switch Channels**
- **2A Primary Channels Can Be Buck, Boost, SEPIC, ZETA, Flyback or Inverting DC/DC Converter**
- **500mA Skyhook Channel Efficiently Generates Boosted Input Voltage**
- **Wide Input Voltage Range of 2.6V to 50V**
- **UVLO and OVLO Programmable on OV/UV Pin**
- Soft-Start Programmable for Each Channel
- Fixed Frequency PWM (Set by RT Pin or Synchronized to External Clock)
- Anti-Phase Switching Reduces Input Ripple
- 20-Lead TSSOP and 28-Lead QFN Packages

APPLICATIONS

- Dual Rail Power for Signal Chain.
- Buck/Buck, Buck/Boost, Boost/Boost, Boost/Invert, Invert/Invert, Buck/Invert

DESCRIPTION

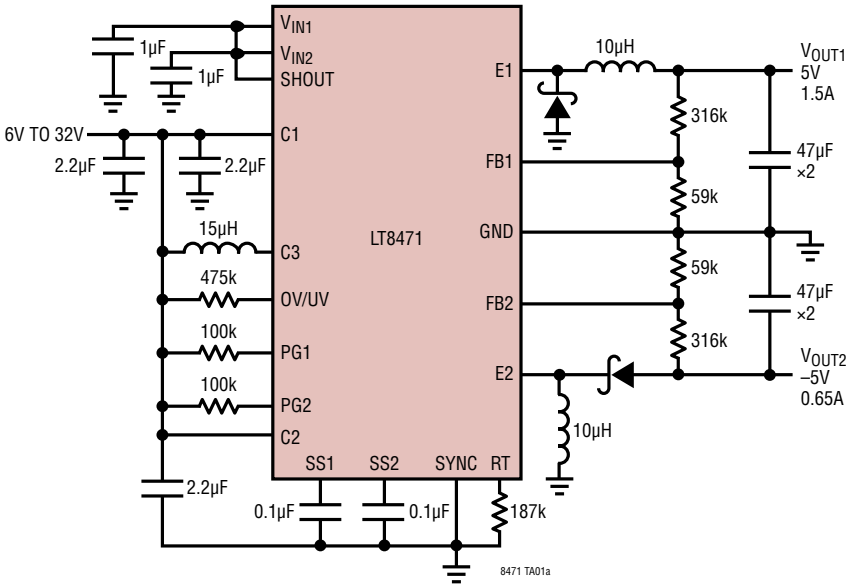
LT8471EUFD is a dual PWM DC/DC converter containing two internal 2A, 50V switches and an additional 500mA switch to facilitate step-down and inverting conversion. Each 2A channel can be independently configured as a buck, boost, SEPIC, flyback or inverting converter. Capable of generating positive and negative outputs from a single input rail, the LT8471 is ideal for many local power supply designs.

The LT8471 has an adjustable oscillator, set by a resistor placed from the RT pin to ground. Additionally, the LT8471 can be synchronized to an external clock. The free running or synchronized switching frequency range of the part can be set between 100kHz and 2MHz.

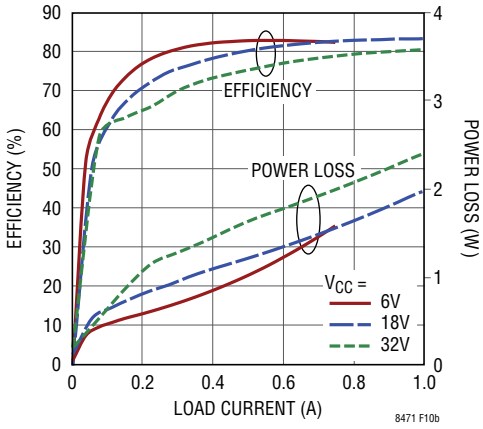
Additional features such as frequency foldback, soft-start, and power good are integrated. The LT8471 is available in 20-lead TSSOP and 28-Lead (4mm × 5mm) QFN packages.

TYPICAL APPLICATION

6V to 32V to ±5V, Dual DC/DC Converter



Efficiency and Power Loss Load from V_{OUT1} to V_{OUT2}

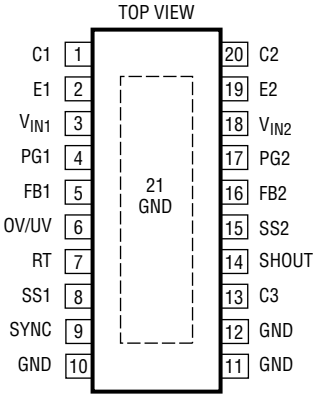


ABSOLUTE MAXIMUM RATINGS

(Note 1)

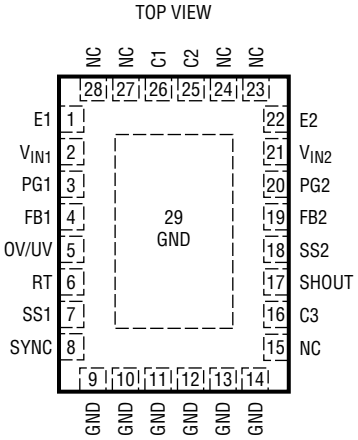
V_{IN1}, V_{IN2} Voltages ..... –0.3V to 50V
C1, C2 Voltages ..... –0.4V to 50V
E1, E2 Voltages ..... –60V to 50V
V_{C1} to V_{E1} and V_{C2} to V_{E2} Voltages ..... –0.4V to 60V
V_{IN1} to V_{E1} and V_{IN2} to V_{E2} Voltages
  Low Side Configurations (Note 6) ..... –0.4V to 40V
  High Side Configurations (Note 6) ..... –0.4V to 60V
V_{IN1} to V_{C1} and V_{IN2} to V_{C2} Voltages
  High Side Configurations (Note 6) ..... –0.4V to 40V
C3 Voltage ..... –0.4V to 50V
RT Voltage ..... –0.3V to 5V
SYNC Voltage ..... –0.3V to 5.5V
SS1, SS2 ..... –0.3V to 2.5V
FB1, FB2 Voltages ..... –2.5V to 2.5V
PG1, PG2 Voltages ..... –0.3V to 50V
OV/UV Voltage ..... –0.3V to 5V
SHOUT Voltage ..... –0.3V to 50V
Operating Junction Temperature Range
  LT8471E (Notes 2, 5) ..... –40°C to 125°C
  LT8471I (Notes 2, 5) ..... –40°C to 125°C
  LT8471H (Notes 2, 5) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
  FE Package ..... 300°C

PIN CONFIGURATION



FE PACKAGE
20-LEAD PLASTIC TSSOP

θ_{JA} = 38°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

θ_{JA} = 44°C/W, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8471EFE#PBF	LT8471EFE#TRPBF	LT8471FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT8471IFE#PBF	LT8471IFE#TRPBF	LT8471FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT8471HFE#PBF	LT8471HFE#TRPBF	LT8471FE	20-Lead Plastic TSSOP	–40°C to 150°C
LT8471EUFD#PBF	LT8471EUFD#TRPBF	8471	28-LEAD (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT8471IUFD#PBF	LT8471IUFD#TRPBF	8471	28-LEAD (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = V_{IN2} = 5V, unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage (V_{IN1}, V_{IN2})		●	2.6		50	V
Quiescent Current (V_{IN1}, Skyhook Disabled)	$V_{OV/UV}$ = 1.3V, Not Switching			2.2	3.3	mA
Quiescent Current (V_{IN1}, Skyhook Enabled)	$V_{OV/UV}$ = 1.3V, C3 = 5V, Not Switching			2.4	4	mA
Quiescent Current (V_{IN2})	$V_{OV/UV}$ = 1.3V, Not Switching			29	42	µA
Quiescent Current in Shutdown (V_{IN1} + V_{IN2})	$V_{OV/UV}$ = 0V			0.01	1	µA
Positive Feedback Voltage (FB1, FB2)		●	773	789	805	mV
Negative Feedback Voltage (FB1, FB2)	(LT8471E,I) (LT8471H)	● ●	–806 –806	–788 –788	–770 –767	mV mV
Feedback Pin Bias Current (FB1, FB2)	V_{FB} = Positive Feedback Voltage, Current Out of Pin V_{FB} = Negative Feedback Voltage		 –100	30 0	200 100	nA nA
Error Amp Transconductances	Primary Channels, ΔI = 2µA			70		µmhos
Error Amp Voltage Gains	Primary Channels			95		V/V
Reference Line Regulation	2.6V ≤ V_{IN1} ≤ 50V			0.008	0.05	%/V
Switching Frequency, f_{OSC}	R_T = 46.4k R_T = 732k	● ●	1.55 100	1.8 117	2.05 135	MHz kHz
Switching Frequency in Foldback	All Channels. Compared to Normal f_{OSC}			1/8		Ratio
Switching Frequency Range	Synchronizing	●	100		2000	kHz
SYNC High Level for Sync		●	1.3			V
SYNC Low Level for Sync		●			0.4	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 2V		35		65	%
Recommended Minimum SYNC Ratio f_{SYNC}/f_{OSC}				¾		Ratio
Switching Phase Between Primary Channels	R_T = 46.4k R_T = 732k		170 170		200 200	Deg Deg
Skyhook Boost Voltage	V_{SHOUT} – V_{C2}, Skyhook Enabled		3.0	4.25	5.4	V
Minimum Switch Off-Time	Primary Channels (Note 7) Skyhook Channel (Note 7)			170 100		ns ns
Minimum Switch On-Time	Primary Channels(Note 7) Skyhook Channel (Note 7)			220 30		ns ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = V_{IN2} = 5V, unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch Current Limit (Primary Channels)	Minimum Duty Cycle (Note 3) Maximum Duty Cycle (Notes 3, 4)	● ●	2.1 1.35	2.55 1.8	3.2 2.5	A A
Switch Current Limit (Skyhook)	(Note 3)	●	400	500	600	mA
Primary Switches V_{CESAT}	I_{C1} or I_{C2} = 1.5A			300		mV
Skyhook Switch V_{CESAT}	I_{C3} = 250mA			250		mV
C1, C2 Leakage Current	V_{C1} = V_{C2} = 12V, V_{E1} = V_{E2} = 0V, $V_{OV/UV}$ = 0V, Current into Pin			0.01	1	µA
C3 Leakage Current	V_{C3} = 12V, $V_{OV/UV}$ = 0V			0.01	1	µA
E1, E2 Leakage Current	$V_{OV/UV}$ = 0V, Current Out of Pin V_{C1} = V_{C2} = 20V, V_{E1} = V_{E2} = 5V V_{C1} = V_{C2} = 5V, V_{E1} = V_{E2} = –10V			 0.01 0.01	 1 1	 µA µA
Schottky Reverse Leakage	$V_{REVERSE}$ = 12V $V_{REVERSE}$ = 50V			0.01 0.02	1 2	µA µA
Schottky Forward Voltage	I_{DIODE} = 100mA			650		mV
Start-Up Characteristics						
Soft-Start Charge Current	V_{SS1}, V_{SS2} = 50mV, Current Flows Out of SS1, SS2 Pins	●	5.5	8.5	11.5	µA
OV/UV Current for OVLO	Current into OV/UV Pin. $V_{OV/UV}$ Internally Clamped to 1.37V, Current Rising	●	76	80	84	µA
OV/UV Pin Bias Current	$V_{OV/UV}$ =1V			0.01	0.5	µA
OV/UV Minimum Input Voltage High	Active Mode, OV/UV Rising Active Mode, OV/UV Falling	● ●	1.165 1.13	1.215 1.18	1.265 1.22	V V
OV/UV Input Voltage Low	Shutdown Mode	●			0.3	V
FB Pin Threshold for Power Good (Positive Output Voltage)	FB Rising FB Falling	● ●	715 708	740 730	765 752	mV mV
FB Pin Threshold for Power Good (Negative Output Voltage)	FB Falling FB Rising	● ●	–766 –755	–736 –727	–706 –699	mV mV
PG1, PG2 Voltage Output Low	V_{FB} = 0.6V, I_{PG} = 250µA			0.32	0.6	V
PG1, PG2 Leakage	V_{PG1}, V_{PG2} = 12V, PG Driver Off			0.01	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8471E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8471I is guaranteed over the full –40°C to 125°C. The LT8471H is guaranteed over the full –40°C to 150°C operating junction temperature range. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: Current limit guaranteed by design and/or correlation to static test.

Note 4: Current Limit measured at equivalent switching frequency of 1MHz.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

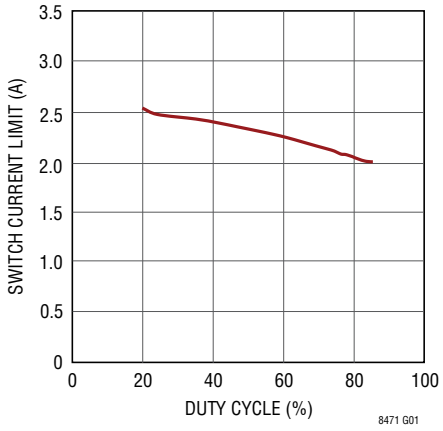
Note 6: Low side and high side configurations are discussed in the Switch Configurations and the Skyhook Regulator section.

Note 7: Minimum switch on-time, off-time is guaranteed by design.

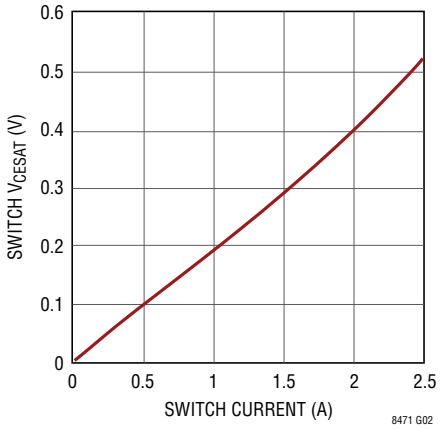
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise specified.

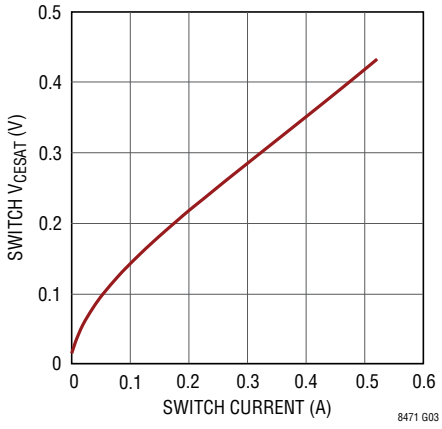
Primary Switch Current Limit at 500kHz



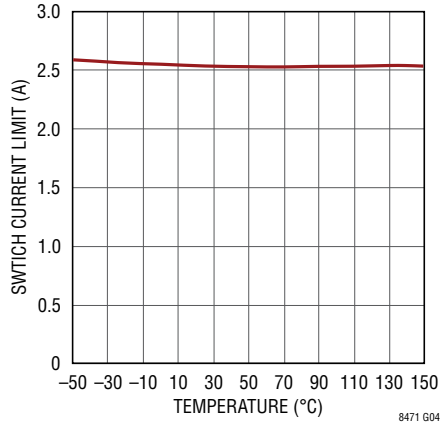
CH1, CH2 Switch V_{CESAT}



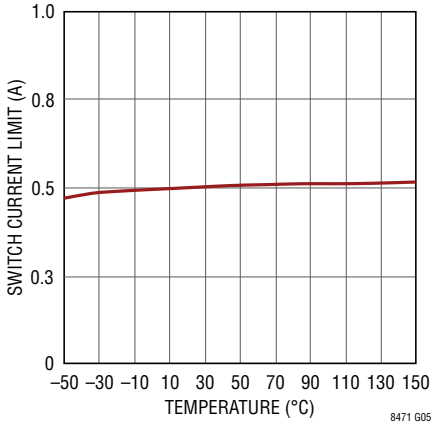
Skyhook Switch V_{CESAT}



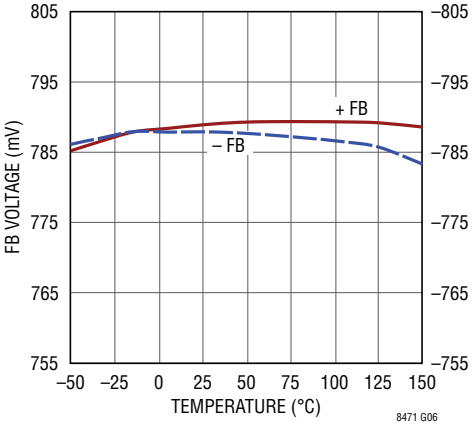
Switch Current Limit at Minimum Duty Cycle



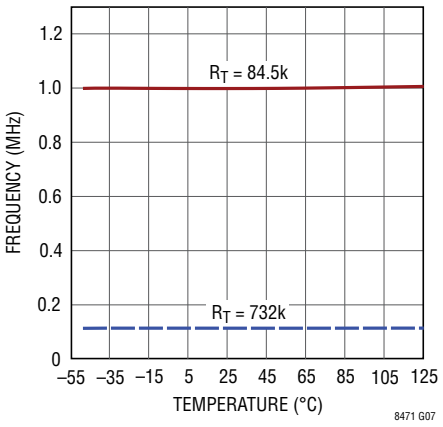
Skyhook Current Limit vs Temperature



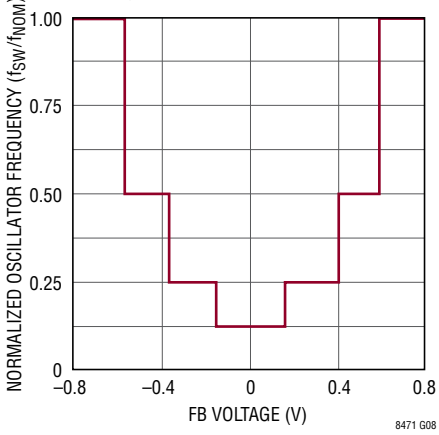
Feedback Voltages



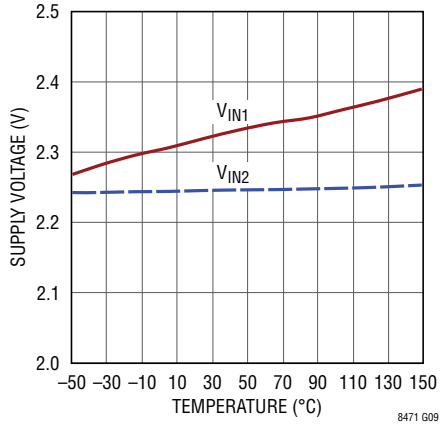
Oscillator Frequency



Switching Frequency During Soft-Start

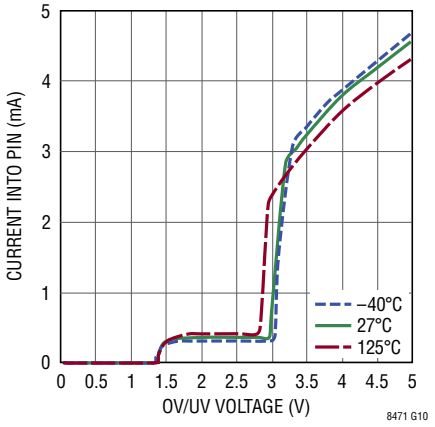


Internal UVLO for V_{IN1} and V_{IN2}

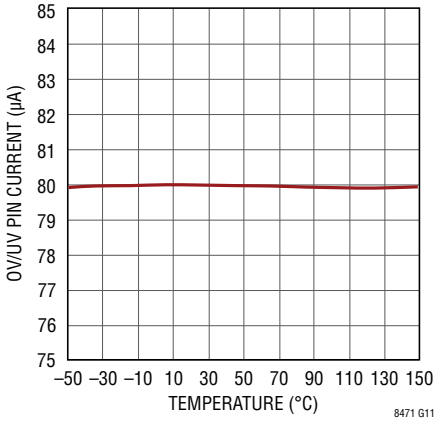


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise specified.

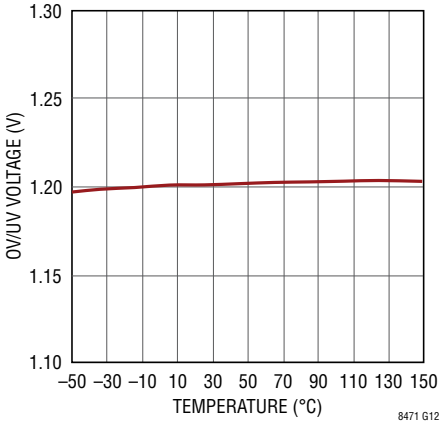
OV/UV Pin Current



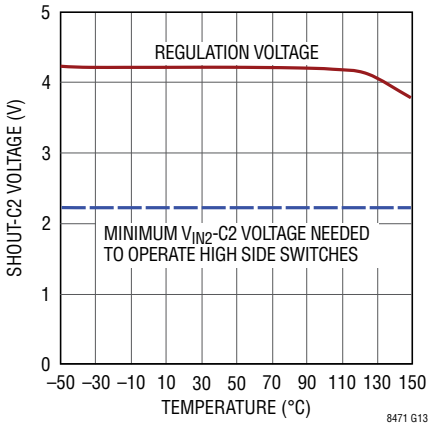
OV/UV Overvoltage Threshold



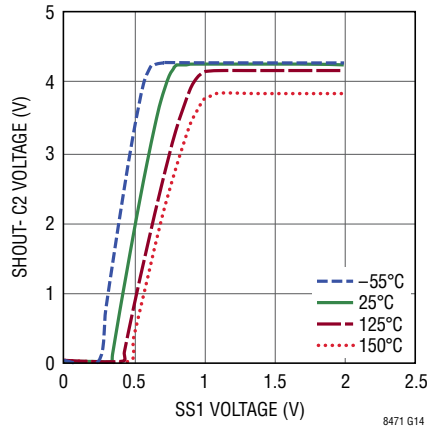
OV/UV Undervoltage Threshold



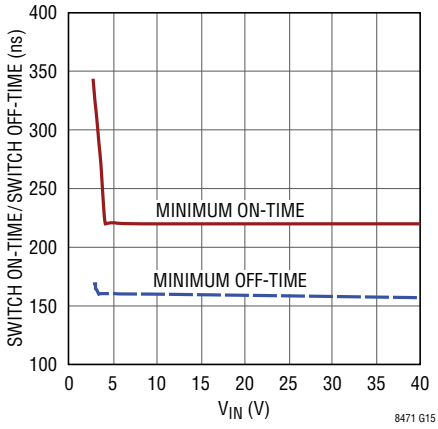
SHOUT-C2 Regulation Voltage vs Temperature



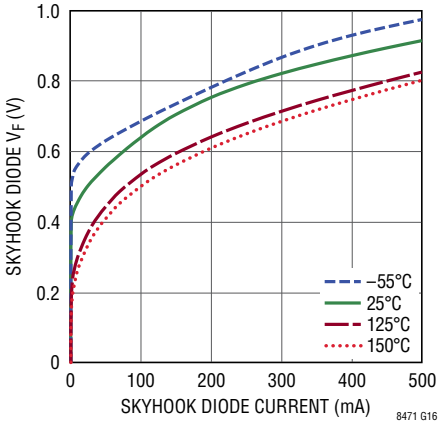
SHOUT-C2 Voltage vs SS1



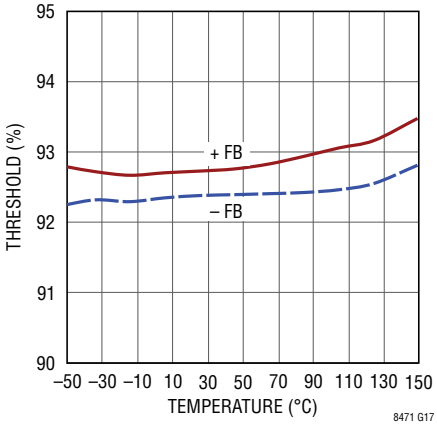
Minimum Switch On-Time/ Switch Off-Time



Skyhook Diode Forward Voltage



PG Threshold vs Temperature (FB Falling)



PIN FUNCTIONS

C1, C2 (Pins 1, 20): Collector Pins. These are the collectors of the primary internal NPN power switches. If either pin is tied to a DC voltage, it must be locally bypassed; if either pin is a switching pin, minimize trace area connected to the pin to minimize EMI. When the Skyhook channel is used, the C2 pin must be tied to the input voltage of the Skyhook channel.

C3 (Pin 13): Skyhook Collector Pin. This is the collector of the internal NPN power switch for the Skyhook channel. If the Skyhook channel is used, minimize the metal trace area connected to this pin to minimize EMI. If the Skyhook channel is not used, tie the C3 pin to GND.

E1, E2 (Pins 2, 19): Emitter Pins. These are the emitters of the primary internal NPN power switches. Unless grounded, minimize trace area connected to these pins to minimize EMI.

FB1, FB2 (Pins 5, 16): Feedback Pins for Primary Channels. Connect a resistor divider between V_{OUT}, FB and GND to set the output voltage.

GND (Pins 10, 11,12, Exposed Pad 21): Ground. All of the ground pins must be soldered directly to the local ground plane. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board.

OV/UV (Pin 6): Overvoltage/Undervoltage Pin. Tie to 1.215V (typical) or more to enable the device; ground to shut down. Configurable as a UVLO and OVLO by connecting to an external resistor divider. See the Applications Information section for more information.

PG1, PG2 (Pins 4, 17): Power Good Pins. Connect pull-up resistors to these pins. These open-drain output pins are pulled low when their respective output voltages are more than 7.5% below their target output voltages (as set by the external feedback resistors). When the output voltage is above 92.5% of the target voltage, the respective PG pin driver turns off, allowing the PG voltage to rise and indicate that the regulated output voltage is good.

RT (Pin 7): Timing Resistor Pin. Adjusts the switching frequency. Place a resistor from this pin to ground to set the frequency to a fixed free-running level. Do not float this pin.

SHOUT (Pin 14): Skyhook Output Voltage Pin. This is the cathode of the internal Schottky diode and the output of the Skyhook boost converter.

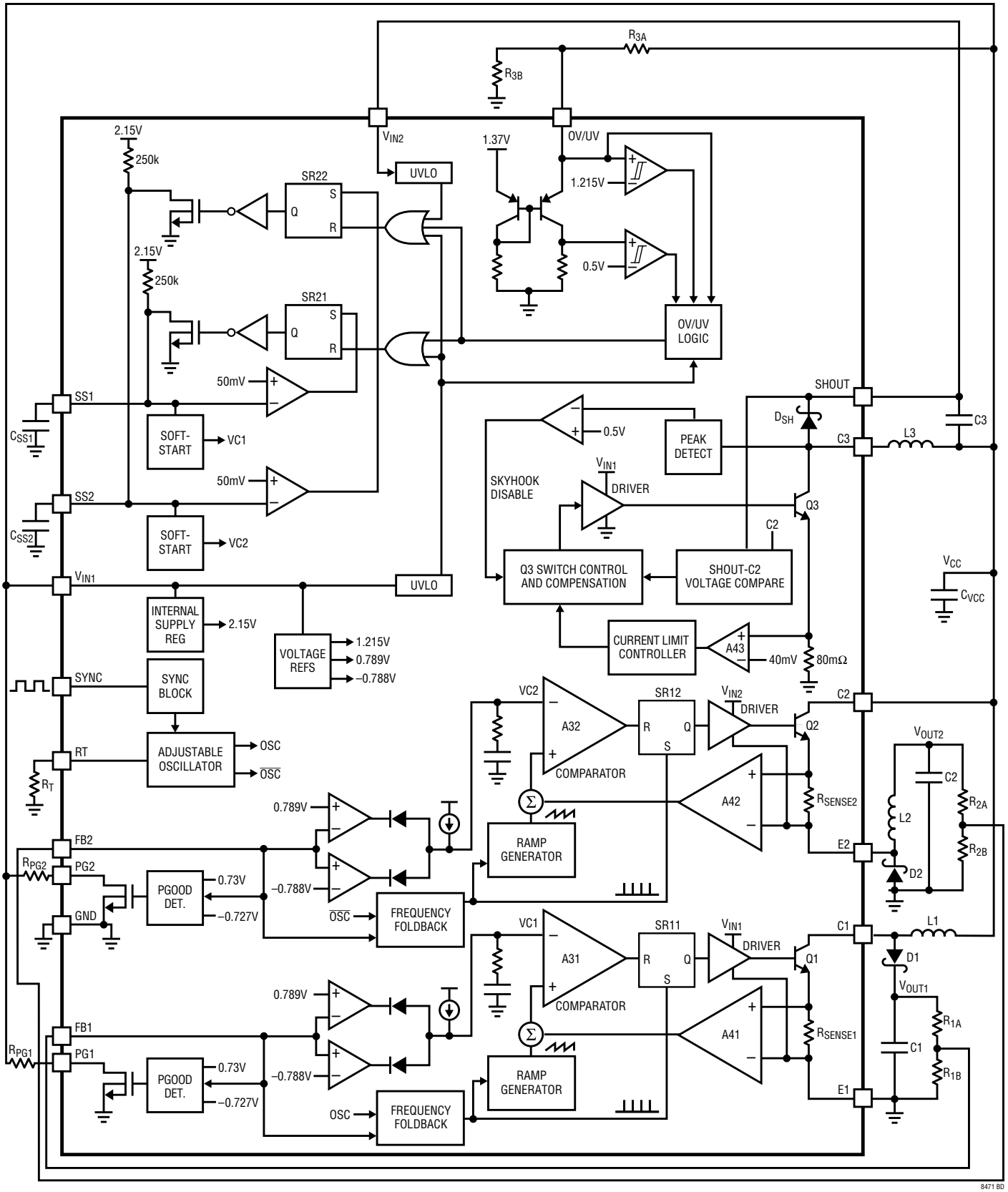
SS1, SS2 (Pins 8, 15): Soft Start Pins. Place a soft-start capacitor on each pin. Upon start-up, the SS pins will be charged by (nominally) 250k resistors to about 2.15V.

SYNC (Pin 9): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock needs to exceed 1.3V, and the low level should be less than 0.4V. Drive this pin to less than 0.4V to revert to the internal free running clock. See the Applications Information section for more information.

V_{IN1} (Pin 3): Input Supply Pin 1. This is the power supply pin for primary channel 1 and the Skyhook channel. This pin also provides power to additional circuitry common to all channels. V_{IN1} must be greater than 2.6V for any channel to operate. V_{IN1} must be locally bypassed.

V_{IN2} (Pin 18): Input Supply Pin 2. This is the power supply pin for primary channel 2 and must be greater than 2.6V when channel 2 is in use. V_{IN2} must be locally bypassed.

BLOCK DIAGRAM



8471 BD

OPERATION

The LT8471 consists of two primary channels, each with a 2A power switch. One Skyhook channel is also available with a 500mA power switch to support the primary channels when performing step-down conversions. The maximum voltage between V_{IN1} and E1 (or V_{IN2} and E2) is 40V when E1 (or E2) is grounded. This is the case for boost, SEPIC, flyback and dual-inductor inverting topologies. The maximum allowed voltage between V_{IN1} and E1 (or V_{IN2} and E2) is 60V when E1 (or E2) is allowed to toggle, such as in buck, ZETA and single-inductor inverting topologies.

Primary Channels

The two primary channels, 1 and 2, can be independently configured as boost, buck, SEPIC, ZETA, flyback or inverting DC/DC converters to adapt into various applications. Both channels use a constant-frequency, current mode control scheme to provide line and load regulation (refer to the Block Diagram). The channel 1 clock is in phase with the internal oscillator or the SYNC pin if it is toggling. In order to reduce transient switching spikes, the clock for channel 2 is approximately 180° out-of-phase with the channel 1 clock.

At the start of each clock phase, an SR latch (SR11/SR12 in the Block Diagram) is set, turning on the internal power switch (Q1/Q2 in the Block Diagram) for the respective channel. An amplifier (A41/A42 in the Block Diagram) and a comparator (A31/A32 in the Block Diagram) monitor the current flowing through the internal power switch, turning the switch off when the current reaches a level determined by the voltage at VC1/VC2. An error amplifier measures the output voltage through an external resistor divider tied to the FB1/FB2 pin and servos the VC1/VC2 voltage. If the error amplifier's output (VC1/VC2) increases, more current is delivered to the output; if it decreases, less current is delivered. An internal clamp on the VC1/VC2 voltage provides current limit.

Both of the primary channels contain a power good comparator which trips when the corresponding FB pin voltage is at 92.5% of its regulated value. The PG1 and PG2 outputs are driven by open-drain N-channel MOSFET devices that are off when the respective output is in regulation, allowing external resistors to pull the PG1/PG2 pins high. The PG1 and PG2 pin states are only valid when the respective channel is enabled and V_{IN1} is above 2.6V.

Skyhook Channel

When either channel is configured as a buck, ZETA or single-inductor inverting converter, the respective V_{IN} pin(s) must be boosted above the input voltage, V_{CC}. The boosted supply provides base current to the appropriate Q1 and/or Q2 NPN power switch. The Skyhook channel provides this boosted voltage to the SHOUT pin which must also be connected to V_{IN2} and/or V_{IN1} as needed.

The Skyhook is a constant-frequency, voltage mode boost converter including a Schottky diode integrated on chip. The Skyhook output, SHOUT, is regulated to a fixed voltage (4.25V typical) above the C2 pin which must be connected to a DC voltage (typically V_{CC}). If the Skyhook is not needed it can be disabled by tying the C3 pin to GND. This also reduces the current draw from V_{IN1}. Refer to the Applications Information section for more information about the proper use of the Skyhook channel.

The Skyhook operates as follows: An error amplifier measures the output voltage (SHOUT) through the SHOUT-C2 voltage comparator and servos an internal control voltage. The control voltage determines the on-time of the Q3 power switch for each cycle, and thus, the amount of current being delivered to SHOUT. Loop compensation is integrated in the chip. Comparator A43 monitors the current in the power switch Q3 in order to detect over current conditions. If current in excess of 500mA (typ) is detected, switch Q3 is immediately turned off.

Start-Up Operation

Several functions are provided to enable a clean start-up for the LT8471.

- First, the OV/UV pin voltage is monitored by an internal voltage reference to give a precise turn-on voltage range. An external resistor (or resistor divider) can be connected from the input power supply to the OV/UV pin to provide a user-programmable undervoltage and overvoltage lockout function.
- Second, the soft-start circuitry provides for a gradual ramp-up of the switch current for the primary channels

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and a gradual ramp-up of duty cycle for the Skyhook channel. When the part is brought out of shutdown, the external SS capacitors are first discharged (providing protection against OV/UV pin glitches and slow ramping). Next, internal 250k resistors pull the SS pins up to ~2.15V. By connecting an external capacitor to each of the SS pins, the voltage ramp rates on the pins can be set. Typical values for the soft-start capacitor range from 100nF to 1µF.

- Finally, the primary channels' switching frequency is folded back by 2, 4, or 8 times when the corresponding FB pin voltage is below certain thresholds (see the Typical Performance Characteristics section). This feature reduces the minimum duty cycle that the part can achieve, thus allowing better control of the switch current during start-up. The slope compensation function is disabled during foldback to increase the available current that can be delivered to the output.

Thermal Shutdown Operation

Not shown in the Block Diagram is the thermal shutdown circuit. If the temperature of the part exceeds approximately 164°C, the SR21 and SR22 latches are set. A full soft-start cycle will then be initiated after the temperature drops below approximately 162.5°C. The thermal shutdown circuit protects the power switches as well as the external components connected to the LT8471.

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Input Supply Requirements

V_{IN1} is the main power supply of the LT8471. It powers channel 1, the Skyhook channel and most of the internal control and bias circuits for both channels. It must be powered up to enable any channel of the LT8471. V_{IN2} is the power supply for channel 2, and only needs to be powered up when channel 2 is used. When V_{IN2} is not powered up, channel 2 will shut down.

Switch Configurations and the Skyhook Regulator

The primary channel NPN power switches can be connected in low side or high side configurations. A low side connection is when the power switch is on the lower voltage side of the inductor while the switch is on. The boost, SEPIC, flyback and dual-inductor inverting configurations use low side power switches. Conversely, a high side connection is when the power switch is on the higher voltage side of the inductor when it is on. The buck, ZETA and single-inductor inverting configurations use high side power switches. Channels 1 and 2 can be configured for high side or low side switching and do not need to be configured in the same way as the other.

In the low side configurations, the E pin is typically tied to ground and the respective C pin toggles. V_{IN} for the respective channel must operate in a range of 2.6V to 40V.

High side configurations require that the C pin be tied to a positive DC voltage supply and the respective E pin toggles. The channel's V_{IN} pin should be at least 2.2V (typical) higher than the respective C pin to provide adequate drive to the base of the NPN power switch. When configured with a high side switch, the channel's V_{IN} can operate up to 50V above ground, 60V above the respective E pin voltage, and 40V above the respective C pin voltage.

The Skyhook boost regulator is available to provide additional V_{IN} voltage when it is needed to support high side switch topologies. When enabled, the Skyhook output voltage (SHOUT) is regulated to 4.25V (typical) above the C2 pin voltage. Figure 1 shows an example where the application input voltage is 6V to 32V. The Skyhook boost converter regulates SHOUT, V_{IN1} and V_{IN2} to 10.25V to 36.25V insuring that the V_{IN1} and V_{IN2} pins are typically 4.25V above the C1 and C2 pins. More information about the Skyhook regulator is available in later sections.

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Internal Undervoltage Lockouts

The LT8471 monitors V_{IN1} and V_{IN2} supply voltages in case either drops below a minimum operating level (typically about 2.35V and 2.25V, respectively).

When V_{IN1} is detected low, all power switches are de-activated, and while sufficient V_{IN1} voltage persists, the soft-start capacitors for both SS1 and SS2 are discharged. After V_{IN1} is detected high, the channel 1 power switch is re-enabled and SS1 begins charging.

When V_{IN2} is detected low, the channel 2 power switch is deactivated, and while sufficient V_{IN1} voltage persists, the soft-start capacitor for SS2 is discharged. After both V_{IN1} and V_{IN2} are detected high, the channel 2 power switch is re-enabled and SS2 begins charging.

Oscillator

The internal free-running oscillator can set the operating frequency of the LT8471. When the SYNC pin is driven low (< 0.4V), the frequency of operation is set by a resistor from RT to ground. An internally trimmed timing capacitor resides inside the IC. The oscillator frequency is calculated using the following formula:

$$f_{OSC} = \frac{85.5}{R_T + 1}$$

where f_{OSC} is in MHz and R_T is in kΩ. Conversely, R_T (in kΩ) can be calculated from the desired frequency (in MHz) using:

$$R_T = \frac{85.5}{f_{OSC}} - 1$$

Clock Synchronization

The operating frequency of the LT8471 can be synchronized to an external clock source. To synchronize to the external source, simply provide a digital clock signal into the SYNC pin. The LT8471 will operate at the SYNC clock frequency. The LT8471 will revert to the internal free-running oscillator clock after SYNC is driven low for a few free-running clock cycles.

Driving SYNC high for an extended period of time effectively stops the operating clock and prevents latches SR11 and SR12 from becoming set (see the Block Diagram). As a result, the switching operation of the LT8471 stops, and all the power switches are turned off.

The duty cycle of the SYNC signal must be between 35% and 65% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

1. SYNC may not toggle outside the frequency range of 100kHz to 2MHz unless it is set low to enable the free-running oscillator.
2. The SYNC frequency can always be higher than the free-running oscillator frequency, f_{OSC}, but should not be less than 25% below f_{OSC}.

Operating Frequency Selection

There are several considerations in selecting the operating frequency of the converter. The first is staying clear of sensitive frequency bands, which cannot tolerate any spectral noise. For example, in products incorporating RF communications, the 455kHz IF frequency is sensitive to any noise, therefore switching above 600kHz is desired. Some communications have sensitivity to 1.1MHz, and in that case, a 1.5MHz switching converter frequency may be employed. The second consideration is the physical size of the converter. As the operating frequency goes up, the inductor and filter capacitors go down in value and size. The trade-off is efficiency, since the switching losses due to NPN base charge (see the Power and Thermal Calculation section), Schottky diode charge, and other capacitive loss terms increase proportionally with frequency.

Soft-Start

The LT8471 contains soft-start circuitry to limit peak switch currents during start-up. High start-up current is inherent in switching regulators since the feedback loop is saturated due to V_{OUT} being far from its final value. The regulator tries to charge the output capacitor as quickly as possible, which results in large peak currents.

The start-up current can be limited by connecting external capacitors (typically 100nF to 1µF) to the SS1 and SS2 pins. The capacitors are slowly charged to ~2.15V by internal

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250k resistors after the part is activated. SS1 pin voltages below ~0.8V reduce the duty cycle of the Skyhook channel, and below ~1.4V reduce the current limit of channel 1. SS2 voltages below ~1.4V reduce the current limit of channel 2. Thus, the gradual ramping of the SS voltages also gradually increases the current limits of the primary channels and the duty cycle of the Skyhook channel. This, in turn, allows the output capacitors for each channel to charge gradually toward its final value while limiting the start-up currents.

In the event of a shutdown (OV/UV pin), internal undervoltage lockout (UVLO) or a thermal lockout, the soft-start capacitors are automatically discharged to <50mV before charging resumes, assuring that the soft-starting occurs after every reactivation of the chip.

Shutdown

The OV/UV pin is used to enable and disable the chip. When configured properly, the OV/UV pin can serve as both an undervoltage and an overvoltage detector as discussed further in the next section. When the OV/UV voltage is below 1.215V (typ) switching activity is disabled as shown in Figure 1 (lockout state). When OV/UV is below 300mV, quiescent current becomes very low and the part is completely in shutdown. Voltages between 1.215V and 1.37V enable the part (ACTIVE state) for normal operation. The OV/UV pin is internally clamped to approximately 1.37V and should always be connected through a resistor to limit the current. If the OV/UV pin current exceeds 80µA (typ), switching is disabled and the part enters the lockout state. See the OV/UV pin current graph in the Typical Performance Characteristics section.

When in the lockout state, the power switches are disabled and the SR21 and SR22 latches are set. This causes the soft-start capacitors to discharge until active operation is enabled. Although the power switches are disabled, the lockout state does not necessarily reduce quiescent current until the OV/UV voltage is near or below the shutdown threshold.

Due to the 1.37V clamping circuit, OV/UV should always be connected through a resistor to limit the current. If the over and undervoltage functions are not used, the OV/UV pin can be driven digitally through a current limiting resistor.

Figure 2 shows how to configure an overvoltage lockout (OVLO) and/or undervoltage lockout (UVLO) for the

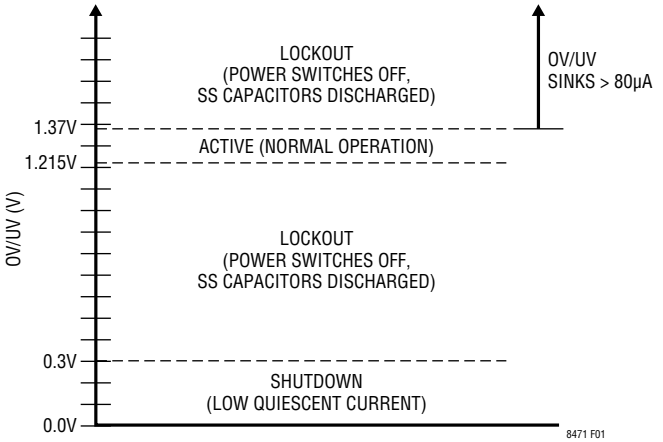

Figure 1. Chip States vs OV/UV Voltage

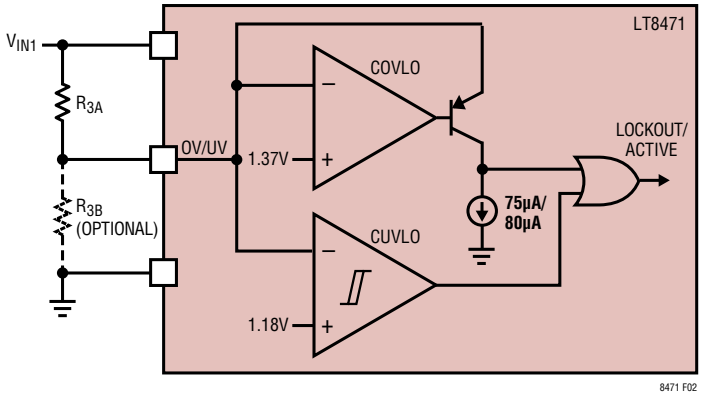

Figure 2. Configurable OVLO and UVLO

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LT8471. Comparator CUVLO detects undervoltage conditions by comparing the OV/UV pin to typical thresholds of 1.215V (rising) and 1.18V (falling). The COVLO comparator detects over voltage conditions by comparing the OV/UV pin current to typical thresholds of 80µA (rising) and 75µA (falling).

Possible reasons to use the UVLO and/or OVLO functions are as follows: A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current-limit or latch up under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where these problems might occur. The OVLO function is used to stop the switching regulator(s) in cases where the input supply voltage overshoots higher than desired.

As an example, V_{IN1} overvoltage and undervoltage thresholds can be set independently by properly choosing R_{3A} and R_{3B}. Use the following formulas to determine the resistor values:

$$R_{3A} = \left(\frac{V_{OVLO+}}{80\mu A}\right) - \left(\frac{1.37 \bullet V_{UVLO-}}{1.18 \bullet 80\mu A}\right)$$

$$R_{3B} = \left(\frac{1.18}{V_{UVLO-} - 1.18}\right) \bullet R_{3A}$$

where:

V_{OVLO+} is the desired rising OVLO threshold

V_{UVLO-} is the desired falling UVLO threshold

After R_{3A} and R_{3B} have been selected, the UVLO and OVLO rising and falling thresholds can be determined using:

$$V_{OVLO+} = 1.37 \bullet \left(\frac{R_{3A} + R_{3B}}{R_{3B}}\right) + 80\mu A \bullet R_{3A}$$

$$V_{OVLO-} = 1.37 \bullet \left(\frac{R_{3A} + R_{3B}}{R_{3B}}\right) + 75\mu A \bullet R_{3A}$$

$$V_{UVLO+} = 1.215 \bullet \left(\frac{R_{3A} + R_{3B}}{R_{3B}}\right)$$

$$V_{UVLO-} = 1.18 \bullet \left(\frac{R_{3A} + R_{3B}}{R_{3B}}\right)$$

where:

V_{OVLO+} and V_{OVLO-} are the rising and falling OVLO thresholds, respectively.

V_{UVLO+} and V_{UVLO-} are the rising and falling UVLO thresholds, respectively.

There are a few limitations in selecting the OVLO and UVLO threshold voltages.

1. The UVLO threshold must be at least 2.6V so that it's higher than the minimum operating voltage the input supply. If the UVLO function is not needed, R_{3B} can be omitted and R_{3A} can be calculated using:

$$R_{3A} = \left(\frac{V_{OVLO+} - 1.37V}{80\mu A}\right)$$

2. The following relationship must be satisfied:

$$\frac{V_{OVLO+}}{V_{UVLO-}} > \frac{1.37}{1.18} = 1.161$$

As the ratio of V_{OVLO} to V_{UVLO} gets closer to 1.161, the required resistances for R_{3A} and R_{3B} become smaller, thus increasing the operating current.

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The following example shows how to select R_{3A} and R_{3B} to disable the LT8471 for V_{IN1} voltages below 5V and above 15V.

First, check that the ratio of the OVLO to the UVLO threshold is greater than 1.161. Here, the ratio is 15V/5V = 3V, which satisfies the second rule just mentioned.

Next, calculate:

$$R_{3A} = \frac{15V}{80\mu A} - \frac{1.37 \bullet 5V}{1.18 \bullet 80\mu A} = 114.9k$$

Choose R_{3A} to be a standard value resistance of 118k. Next, calculate:

$$R_{3B} = \left(\frac{1.18V}{5V - 1.18V}\right) \bullet 118k = 36.5k$$

Choose R_{3B} to be a standard value resistance of 36.5k.

After selecting the standard value resistors for R_{3A} and R_{3B}, calculate the final thresholds using the formulas previously provided.

$$V_{OVLO}+ = 1.37 \bullet \left(\frac{118k + 36.5k}{36.5k}\right) + 80\mu A \bullet 118k$$
$$= 15.24V$$

$$V_{OVLO}- = 1.37 \bullet \left(\frac{118k + 36.5k}{36.5k}\right) + 75\mu A \bullet 118k$$
$$= 14.65V$$

$$V_{UVLO}+ = 1.215 \bullet \left(\frac{118k + 36.5k}{36.5k}\right) = 5.14V$$

$$V_{UVLO}- = 1.18 \bullet \left(\frac{118k + 36.5k}{36.5k}\right) = 4.99V$$

Setting the Output Voltage (Primary Channels)

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose 1% or better resistors according to:

$$R_A = R_B \bullet \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} is the feedback voltage (0.789V typical for positive V_{OUT} and –0.788V for negative V_{OUT}). Reference designators are as shown in the Block Diagram.

For example, for V_{OUT} = 10V, choose R_{1B} = 10k, then choose:

$$R_{1A} = 10k \bullet \left(\frac{10V}{0.789V} - 1\right) \simeq 115k$$

Start-Up Sequencing

Connecting one primary channel's PG pin to the other channel's SS pin is an easy way to sequence the start-up order of the outputs. For example, in most applications, connecting PG1 to SS2 will make the channel 1 output come up before the channel 2 output during the start-up. Because the skyhook channel does soft-start with the SS1 pin (see more details in the Soft-Start section), the following guidelines need to be applied if both power-up sequencing and the skyhook channel are used:

1. Connect PG1 directly to SS2 to make channel 1's output come up first (see Figure 12).
2. Connect a 147k resistor between PG2 and SS1 to make channel 2's output come up first.

An example using a 147k resistor connected between PG2 and SS1 is shown in Figure 9a. In this application, channel 1 is configured as a boost converter, and channel 2 is configured as a buck converter. The buck converter has to start up first as its output is connected to the input of the boost converter.

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Power Switch Duty Cycle (Primary Channels)

In order to maintain loop stability and deliver adequate current to the load, the internal power switches (Q1 and Q2 in the Block Diagram) cannot remain on for 100% of each clock cycle. The maximum allowable duty cycle is given by:

$$DC_{MAX} = \left(\frac{T_P - MIN_{(OFF)TIME}}{T_P}\right) \bullet 100\%$$

where T_P is the clock period and $MIN_{(OFF)TIME}$ is typically 170ns (refer to the Electrical Characteristics section).

The application should be designed so that the steady state duty cycle does not exceed DC_{MAX}. Duty cycle equations for several common topologies are given below, where V_D is the diode forward voltage drop and V_{CESAT} is typically 300mV at 1.5A.

$$DC_{BOOST} \cong \frac{V_{OUT} - V_{CC} + V_D}{V_{OUT} + V_D - V_{CESAT}}$$

$$DC_{BUCK} \cong \frac{V_{OUT} + V_D}{V_{CC} + V_D - V_{CESAT}}$$

$$DC_{1L\_INV} \cong \frac{|V_{OUT}| + V_D}{V_{CC} + V_D - V_{CESAT} + |V_{OUT}|}$$

$$DC_{2L\_INV} \cong \frac{|V_{OUT}| + V_D}{V_{CC} + V_D - V_{CESAT} + |V_{OUT}|}$$

$$DC_{SEPIC} \cong \frac{V_D + V_{OUT}}{V_{CC} + V_{OUT} + V_D - V_{CESAT}}$$

$$DC_{ZETA} \cong \frac{V_D + V_{OUT}}{V_{CC} + V_{OUT} + V_D - V_{CESAT}}$$

where V_{CC} is the positive input voltage to the DC/DC converter. See the Typical Applications section for examples.

The LT8471 can be used in configurations where the duty cycle is higher than DC_{MAX}, but it must be operated in the discontinuous conduction mode so that the effective duty cycle is reduced.

Inductor Selection (Primary Channels)

General Guidelines: The high frequency operation of the LT8471 allows for the use of small surface mount inductors. For high efficiency, choose inductors with high frequency core material, such as ferrite, to reduce core losses. To improve efficiency, choose inductors with more volume for a given inductance. The inductor should have low DCR (copper wire resistance) to reduce I^2R losses, and must be able to handle the peak inductor current without saturating. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology, where each inductor only carries a fraction of the total switch current. Molded chokes or chip inductors usually do not have enough core area to support peak inductor currents in the 2A to 3A range. To minimize radiated noise, use a toroidal or shielded inductor. Note that the inductance of shielded core types will drop more as current increases, and will saturate more easily. See Table 1 for a list of inductor manufacturers. Thorough lab evaluation is recommended to verify that the following guidelines properly suit the final application.

Table 1. Inductor Manufacturers

VENDOR	PART NUMBER	WEB
Coilcraft	MSS1038, MSS7341 and LPS4018	www.coilcraft.com
Coiltronics	DR, LD and CD Series	www.coiltronics.com
Sumida	CDRH105R Series	www.sumida.com
Würth Elektronik	WE-LHMI and WE-TPC Series	www.we-online.com

Minimum Inductance: Although there can be a trade-off with efficiency, it is often desirable to minimize board space by choosing smaller inductors. When choosing an inductor, there are two conditions that limit the minimum inductance; (1) providing adequate load current, and (2) avoiding subharmonic oscillation. Choose an inductance that is high enough to meet both of these requirements.

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Adequate Load Current: Small value inductors result in increased ripple currents and thus, due to the limited peak switch current, decrease the average current that can be provided to a load (I_{OUT}). In order to provide adequate load current, L should be at least:

$$L_{BOOST} > \frac{DC \bullet V_{CC}}{2 \bullet f \bullet \left(I_{LIM} - \frac{V_{OUT} \bullet I_{OUT}}{V_{CC} \bullet \eta} \right)}$$

$$L_{BUCK} > \frac{DC \bullet (V_{CC} - V_{OUT})}{2 \bullet f \bullet \left(I_{LIM} - \frac{V_{OUT} \bullet I_{OUT}}{V_{CC} \bullet \eta} \right)}$$

$$L_{SEPIC} > \frac{DC \bullet V_{CC}}{2 \bullet f \bullet \left(I_{LIM} - \frac{V_{OUT} \bullet I_{OUT}}{V_{CC} \bullet \eta} - I_{OUT} \right)}$$

$$L_{1L\_INV} > \frac{DC \bullet V_{CC}}{2 \bullet f \bullet \left(I_{LIM} - \frac{|V_{OUT}| \bullet I_{OUT}}{V_{CC} \bullet \eta} \right)}$$

$$L_{2L\_INV} > \frac{DC \bullet V_{CC}}{2 \bullet f \bullet \left(I_{LIM} - \frac{|V_{OUT}| \bullet I_{OUT}}{V_{CC} \bullet \eta} - I_{OUT} \right)}$$

$$L_{ZETA} > \frac{DC \bullet V_{CC}}{2 \bullet f \bullet \left(I_{LIM} - \frac{|V_{OUT}| \bullet I_{OUT}}{V_{CC} \bullet \eta} - I_{OUT} \right)}$$

where:

L = L1||L2 for dual uncoupled inductor topologies.

L = L1 = L2 for dual-coupled inductor topologies.

DC = Switch duty cycle in steady state.

I_{LIM} = Switch current limit, typically about 2.3A at 50% duty cycle (see the Typical Performance Characteristics section).

η = Power conversion efficiency (typically 88% for boost, 75% for dual inductor, 85% for buck and 80% for 1L inverting topologies at high currents).

V_{CC} = Positive input voltage to the DC/DC converter. See the Typical Applications section for examples.

f = Switching frequency.

Negative values of L indicate that the output load current I_{OUT} exceeds the switch current limit capability of the LT8471.

Avoiding Subharmonic Oscillations: The LT8471's internal slope compensation circuit will prevent subharmonic oscillations that can occur when the duty cycle is greater than 50%, provided that the inductance exceeds a minimum value. In applications that operate with duty cycles greater than 50%, the inductance must be at least:

$$L_{BOOST} > \frac{V_{CC} \bullet (2 \bullet DC - 1)}{(1 - DC) \bullet f}$$

$$L_{SEPIC} > \frac{V_{CC} \bullet (2 \bullet DC - 1)}{(1 - DC) \bullet f}$$

$$L_{2L\_INV} > \frac{V_{CC} \bullet (2 \bullet DC - 1)}{(1 - DC) \bullet f}$$

$$L_{BUCK} > \frac{V_{CC} \bullet (2 \bullet DC - 1)}{f}$$

$$L_{1L\_INV} > \frac{V_{CC} \bullet (2 \bullet DC - 1)}{(1 - DC) \bullet f}$$

$$L_{ZETA} > \frac{V_{CC} \bullet (2 \bullet DC - 1)}{(1 - DC) \bullet f}$$

where:

L = L1||L2 for dual uncoupled inductor topologies.

L = L1 = L2 for dual-coupled inductor topologies.

DC = Switch duty cycle in steady state.

V_{CC} = Positive input voltage to the DC/DC converter. See the Typical Applications section for examples.

f = Switching frequency.

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Maximum Inductance: Excessive inductance can reduce current ripple to levels that are difficult for the current comparator (A3 in the Block Diagram) to easily distinguish, thus causing duty cycle jitter and/or poor regulation. The maximum inductance can be calculated using:

$$L_{MAX} = \frac{V_{CC} - V_{CESAT}}{I_{MIN(RIPPLE)} \bullet f} \bullet DC$$

for inverting, boost, ZETA and SEPIC topologies, or:

$$L_{MAX} = \frac{(1-DC) \bullet V_{CC} - V_{CESAT}}{I_{MIN(RIPPLE)} \bullet f} \bullet DC$$

for the buck topology.

where:

L_{MAX} = L1||L2 for dual uncoupled inductor topologies.

L_{MAX} = L1 = L2 for dual-coupled inductor topologies.

$I_{(MIN)RIPPLE}$ is typically 120mA.

DC = Switch duty cycle in steady state.

V_{CC} = Positive input voltage to the DC/DC converter. See the Typical Applications section for examples.

f = Switching frequency.

Maximum Current Rating: Finally, the inductor(s) must be rated to handle the peak operating current to prevent inductor saturation resulting in efficiency loss. In steady state, the peak input inductor current (continuous conduction mode only) is given by:

$$I_{L\_PEAK} = \frac{|V_{OUT} \bullet I_{OUT}|}{V_{CC} \bullet \eta} + \frac{(V_{CC} - V_{CESAT}) \bullet DC}{2 \bullet L \bullet f} \text{ (BOOST)}$$

$$I_{L\_PEAK} = \frac{|V_{OUT} \bullet I_{OUT}|}{V_{CC} \bullet \eta} + \frac{(V_{CC} - V_{CESAT}) \bullet DC}{2 \bullet L \bullet f} \text{ (1L\_INV)}$$

$$I_{L\_PEAK} = I_{OUT} + \frac{(V_{CC} - V_{CESAT}) \bullet DC \bullet (1-DC)}{2 \bullet L \bullet f} \text{ (BUCK)}$$

$$I_{L1\_PEAK} = \frac{|V_{OUT} \bullet I_{OUT}|}{V_{CC} \bullet \eta} + \frac{(V_{CC} - V_{CESAT}) \bullet DC}{2 \bullet L1 \bullet f} \text{ (SEPIC)}$$

$$I_{L2\_PEAK} = I_{OUT} + \frac{(V_{OUT} + V_D) \bullet (1-DC)}{2 \bullet L2 \bullet f} \text{ (SEPIC)}$$

$$I_{L1\_PEAK} = \frac{|V_{OUT} \bullet I_{OUT}|}{V_{CC} \bullet \eta} + \frac{(V_{CC} - V_{CESAT}) \bullet DC}{2 \bullet L1 \bullet f} \text{ (2L\_INV)}$$

$$I_{L2\_PEAK} = I_{OUT} + \frac{(|V_{OUT}| + V_D) \bullet (1-DC)}{2 \bullet L2 \bullet f} \text{ (2L\_INV)}$$

$$I_{L1\_PEAK} = \frac{|V_{OUT} \bullet I_{OUT}|}{V_{CC} \bullet \eta} + \frac{(V_{CC} - V_{CESAT}) \bullet DC}{2 \bullet L1 \bullet f} \text{ (ZETA)}$$

$$I_{L2\_PEAK} = I_{OUT} + \frac{(|V_{OUT}| - V_D) \bullet (1-DC)}{2 \bullet L_2 \bullet f} \text{ (ZETA)}$$

Note that the inductor current can be higher during load transients. It can also be higher during start-up if inadequate soft-start capacitance is used.

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Capacitor Selection (Primary Channels)

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they have an extremely low ESR and are available in very small packages. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wider voltage and temperature ranges. A 4.7µF to 20µF output capacitor is sufficient for most applications, but systems with very low output currents may need only a 1µF or 2.2µF output capacitor. Always use a capacitor with a sufficient voltage rating. Many capacitors rated at 2.2µF to 20µF, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired output voltage. Solid tantalum or OS-CON capacitors can be used, but they will occupy more board area than ceramic ones and will have higher ESR with greater output ripple.

Low ESR capacitors should also be used as the input decoupling capacitors, which should be placed as closely as possible to the LT8471. Ceramic capacitors make a good choice for this purpose. A 2.2µF to 4.7µF input capacitor is sufficient for most applications.

Table 2 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers for detailed information on their entire selection of ceramic capacitors.

Table 2. Ceramic Capacitor Manufacturers

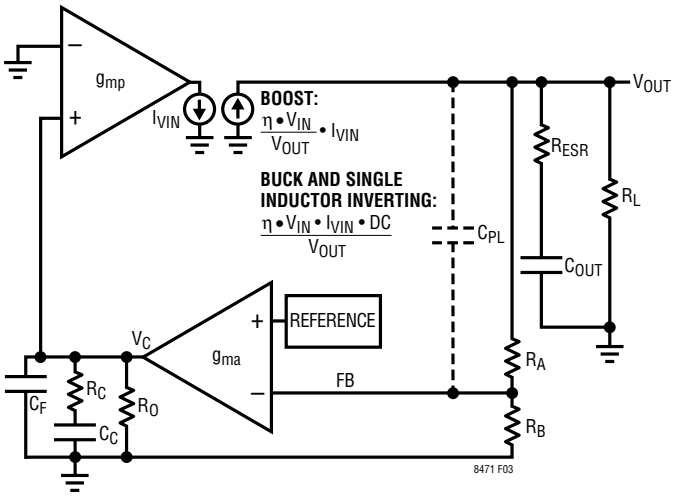
VENDOR	WEB
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo-Yuden	www.t-yuden.com
TDK	www.tdk.com

Compensation Theory (Primary Channels)

Like all other current mode switching regulators, the primary channels of LT8471 need to be compensated for stable and efficient operation. For each primary channel, two feedback loops are used—a fast current loop which does not require compensation, and a slower voltage loop which does. In order to reduce the PCB footprint, the voltage loop compensation network is integrated inside the LT8471. Therefore, only the inductor and the output capacitor are available for adjusting the loop stability. Standard bode plot analysis can be used to analyze and adjust the voltage feedback loop.

As with any feedback loop, identifying the gain and phase contribution of the various elements in the loop is critical. Figure 3 shows the key equivalent elements of a boost/buck/inverting converter. Because of the fast current control loop, the power stage of the IC, inductor and diode have been replaced by a combination of the equivalent transconductance amplifier g_{mp} and the current controlled current source (which converts I_{VIN} to $\eta \bullet V_{IN} \bullet I_{VIN}/V_{OUT}$ for boost converters, I_{VIN} to $\eta \bullet V_{IN} \bullet DC/V_{OUT}$ for buck and single inductor inverting converters). g_{mp} acts as a current source where the peak input current, I_{VIN}, is proportional to the VC voltage. η is the efficiency of the switching regulator, and is typically about 88%.

Note that the maximum output currents of g_{mp} and g_{ma} are finite. The limits for g_{mp} are in the Electrical Characteristics section (switch current limit), and g_{ma} is nominally limited to about ±5µA.



C_C: COMPENSATION CAPACITOR
C_{OUT}: OUTPUT CAPACITOR
C_{PL}: PHASE LEAD CAPACITOR
g_{ma}: TRANSCONDUCTANCE AMPLIFIER INSIDE IC
g_{mp}: POWER STAGE TRANSCONDUCTANCE AMPLIFIER
R_C: COMPENSATION RESISTOR
R_L: OUTPUT RESISTANCE DEFINED AS V_{OUT} DIVIDED BY $I_{LOAD(MAX)}$
R_O: OUTPUT RESISTANCE OF g_{ma}
R_A, R_B: FEEDBACK RESISTOR DIVIDER NETWORK
R_{ESR}: OUTPUT CAPACITOR ESR

Figure 3. Boost/Buck/Inverting Converter Equivalent Model

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From Figure 3, the DC gain, poles and zeros can be calculated as follows:

DC Gain:

Boost Converters:

$$A_{DC} = (g_{ma} \bullet R_O) \bullet g_{mp} \bullet \left(\eta \bullet \frac{V_{IN}}{V_{OUT}} \bullet \frac{R_L}{2} \right) \bullet \frac{R_B}{R_A + R_B}$$

Buck Converters:

$$A_{DC} = (g_{ma} \bullet R_O) \bullet g_{mp} \bullet (\eta \bullet R_L) \bullet \frac{R_B}{R_A + R_B}$$

Single Inductor Inverting Converters:

$$A_{DC} = (g_{ma} \bullet R_O) \bullet g_{mp} \bullet \left(\eta \bullet \frac{V_{IN}}{V_{IN} + 2 \bullet |V_{OUT}|} \bullet R_L \right) \bullet \frac{R_B}{R_A + R_B}$$

Output Pole:

Boost Converters: $P1 = \frac{2}{2 \bullet \pi \bullet R_L \bullet C_{OUT}}$

Buck Converters: $P1 = \frac{1}{2 \bullet \pi \bullet R_L \bullet C_{OUT}}$

Single Inductor Inverting Converters:

$$P1 = \frac{2 \bullet |V_{OUT}| + V_{IN}}{2 \bullet \pi \bullet R_L \bullet C_{OUT} \bullet \left(V_{IN} + |V_{OUT}| \right)}$$

Error Amp Pole: $P2 = \frac{1}{2 \bullet \pi \bullet R_O \bullet C_C}$

Error Amp Zero: $Z1 = \frac{1}{2 \bullet \pi \bullet R_C \bullet C_C}$

ESR Zero: $Z2 = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}}$

High Frequency Pole: $P3 > \frac{f_S}{3}$

Phase Lead Zero: $Z4 = \frac{1}{2 \bullet \pi \bullet R_A \bullet C_{PL}}$

Phase Lead Pole: $P4 = \frac{1}{2 \bullet \pi \bullet C_{PL} \bullet \frac{R_A \bullet R_B}{R_A + R_B}}$

Error Amp Filter Pole:

$$P5 = \frac{1}{2 \bullet \pi \bullet \frac{R_C \bullet R_O}{R_C + R_O} \bullet C_F}, C_F < \frac{C_C}{10}$$

RHP Zero:

Boost Converters: $Z3 = \frac{(1 - DC)^2 \bullet R_L}{2 \bullet \pi \bullet L}$

Buck Converters: $Z3 = \infty$

Single Inductor Inverting Converters:

$$Z3 = \frac{(1 - DC)^2 \bullet R_L}{2 \bullet \pi \bullet DC \bullet L}$$

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Using the primary channel 1 in Figure 11a as an example, Table 3 shows the parameters used to generate the bode plot shown in Figure 4.

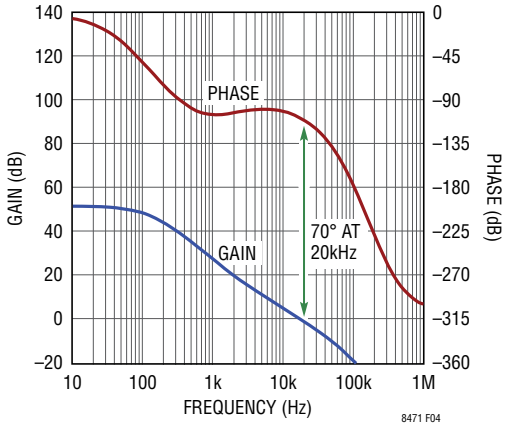

Figure 4. Bode Plot for Example Buck Converter

In Figure 4, the phase is –110° when the gain reaches 0dB, giving a phase margin of 70°. The crossover frequency is 20kHz.

Table 3. Bode Plot Parameters

PARAMETER	VALUE	UNITS	COMMENT
R_L	3.3	Ω	Application Specific
C_{OUT}	94	µF	Application Specific
R_{ESR}	1	mΩ	Application Specific
R_O	1.35	MΩ	Not Adjustable
C_C	1	nF	Not Adjustable
C_F	10	pF	Not Adjustable
C_{PL}	0	pF	Optional/Adjustable
R_C	155	kΩ	Not Adjustable
R_A	319	kΩ	Adjustable
R_B	59	kΩ	Adjustable
V_{OUT}	5	V	Application Specific
V_{IN}	12	V	Application Specific
g_{ma}	70	µmho	Not Adjustable
g_{mp}	7.3	mho	Not Adjustable
L	10	µH	Application Specific
f_S	0.45	MHz	Adjustable

The previous discussion is a good start for narrowing down the range of component values so that the overall design meets the stability requirements. To obtain good stability margin and transient response, some fine tuning of the external components, i.e., the inductor and output capacitor may be necessary.

Diode Selection (Primary Channels)

Schottky diodes, with their low forward-voltage drops and fast switching speeds, are recommended for use with the LT8471. Each of the primary channels need an external diode as the second switch. The diode conducts current only during the switch off-time. The average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = I_{OUT} \bullet (1 - DC)$$

where I_{OUT} is the output load current, and DC is the switch duty cycle in steady state.

Choose a diode rated to handle at least $I_{D(AVG)}$. Diodes with higher current rating should be selected to handle increased current during start-up, load transient and/or output short. Choose a Schottky diode with low parasitic capacitance to reduce reverse current spikes through the power switch of the LT8471. In addition, when operating at high ambient temperatures and with high reverse voltages across the Schottky, choose diodes with lower reverse leakage current to avoid excessive heating in the diode. Table 4 lists several Schottky diodes and their manufacturers.

Table 4. Diode Vendors

PARAMETER	V_R (V)	I_{AVE} (A)	V_F AT 1A (mV)	V_F AT 2A (mV)
Diodes, Inc.				
B120	20	1	500	
B130	30	1	500	
B220	20	2		500
B230	30	2		500
DFLS260L	60	2	410	620
Microsemi				
UPS140	40	1	450	
Fairchild				
SS16	60	1	700	
International Rectifier				
10BQ030	30	1	420	470
20BQ030	30	2		470

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Skyhook Configuration Requirements

The Skyhook provides the boosted V_{IN} voltage required for channels operating in the high side configuration. High side channels have their respective C pin tied to a positive DC voltage supply (usually V_{CC}) while the respective E pin toggles. The channel's V_{IN} pin should be at least 2.2V (typical) higher than the respective C pin to provide adequate base drive for the NPN power switch. Internal circuits monitor the voltage difference between V_{IN1} and E1 (and V_{IN2} and E2). If the voltage difference is less than 2.2V (typical), the power switch will be turned off immediately for that clock cycle. Increasing voltage difference between V_{IN} and the respective C pin increases power loss and reduces efficiency. V_{IN} must not be more than 40V higher than the respective C pin for high side configurations. If use of Skyhook channel is not desired, then the boosted V_{IN} voltage can instead be provided by an external power supply or by the output of the opposite channel if the voltage is high enough.

The Skyhook output (SHOUT) is regulated to ~4.25V above the C2 pin voltage and can be connected to the appropriate V_{IN} pin(s) as shown in the Typical Applications section. When in use, the Skyhook can only be configured as a boost converter (i.e., as in Figure 1a). Also, since SHOUT is regulated to ~4.25V above C2, the C2 pin must be connected to a DC voltage (usually V_{CC}) and must not be toggling. Because of this requirement, if channel 2 is used while the Skyhook is operating, channel 2 must be in the high side configuration such as buck or single-inductor inverting. If not being used, the Skyhook channel can be disabled by connecting the C3 pin to ground. When the Skyhook channel is disabled V_{IN1} current is reduced.

Capacitor and Diode Selection (Skyhook)

A low ESR capacitor should be used at the Skyhook output to minimize voltage ripple. Ceramic capacitors make a good choice for this (see the discussion in the Capacitor Selection (Primary Channels) section). The capacitor value can affect stability. Read the upcoming Compensation (Skyhook) section for more information.

For the best noise performance, the Skyhook output capacitor should be connected from SHOUT to GND, and the capacitors should be placed close to the pins (V_{IN1} or V_{IN2}) that SHOUT is shorted to. The Skyhook output capacitor can also be connected from SHOUT to the C2 pin (usually V_{CC}), as shown in Figure 9a. By doing this, the output voltage of the Skyhook, or the boosted base drive voltage for the primary channels will have better tracking with the supply voltage of the channel. In addition, the voltage across the capacitor is lower, thus reducing the size and required voltage rating of the capacitor.

The Skyhook has a Schottky diode built on-chip. Nevertheless, an external Schottky diode can be connected from C3 to SHOUT to improve performance when load currents are high. The diode choice can be made based on the discussion in the Diode Selection (Primary Channels) section. The output current (I_{OUT}) for the Skyhook channel can be estimated as:

$$I_{OUT} \cong \frac{(V_{CC} + 4.25V) \bullet (I_{OUT1} \bullet DC_1 + I_{OUT2} \bullet DC_2)}{\beta \bullet V_{CC} \bullet \eta}$$

where:

V_{CC} = Input voltage of the Skyhook.

I_{OUT1} = Average output current of channel 1 if V_{IN1} is connected to SHOUT (0 otherwise).

I_{OUT2} = Average output current of channel 1 if V_{IN2} is connected to SHOUT (0 otherwise).

DC1 = Duty cycle of channel 1 in steady state.

DC2 = Duty cycle of channel 2 in steady state.

η = Power conversion efficiency of the Skyhook (typically 87%).

β = Channel 1/channel 2 power switch beta (typically 35)

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Inductor Selection (Skyhook)

The general guidelines are the same as the ones for primary channels, and can be found in the previous section.

Minimum Inductance: There are three conditions that limit the minimum inductance for the Skyhook boost converter:

1. Provide adequate load current;
2. Avoid excessive power switch current overshoot;
3. Maintain good loop stability (see the subsequent Compensation (Skyhook) section).

Choose an inductance that satisfies the minimum requirements for all three criteria. At least 20% of additional margin is recommended for the inductance.

Adequate Load Current: Starting by assuming the Skyhook operates in discontinuous mode (DCM), the minimum inductance ($L_{DCM(MIN)}$) to provide adequate load current is:

$$L_{DCM(MIN)} > \frac{(I_{OUT1} \bullet DC1 + I_{OUT2} \bullet DC2) \bullet 4.25V \bullet 2}{35 \bullet \eta \bullet f \bullet I_{LIM}^{2}}$$

Next, verify if the Skyhook will actually operate in DCM with the following inequality:

$$I_{LIM} \bullet L_{DCM(MIN)} \bullet f \bullet \left(\frac{1}{V_{CC}} + \frac{1}{4.25V} \right) < 1$$

If this inequality is true, then the Skyhook will operate in DCM, and $I_{DCM(MIN)}$ is the minimum inductance needed to provide adequate load current. Otherwise, the Skyhook will operate in continuous mode (CCM) when providing maximum load current, and the minimum inductance ($L_{CCM(MIN)}$) needed is:

$$L_{CCM(MIN)} > \frac{DC_{SH} \bullet V_{CC}}{2 \bullet f \bullet \left(I_{LIM} - \frac{(V_{CC} + 4.25V) \bullet (I_{OUT1} \bullet DC1 + I_{OUT2} \bullet DC2)}{35 \bullet V_{CC} \bullet \eta} \right)}$$

where:

DC_{SH} = Skyhook duty cycle in steady state:

$$DC_{SH} \cong \frac{4.25V + V_{DSH}}{V_{C2} + 4.25V + V_{DSH}}$$

V_{DSH} = Skyhook diode forward voltage drop (see the Electrical Characteristics section).

V_{CC}= Input voltage of the Skyhook.

I_{LIM} = Skyhook switch fault current limit, typically 500mA.

I_{OUT1} = Average output current of channel 1 if V_{IN1} is connected to SHOUT (0 otherwise).

I_{OUT2} = Average output current of channel 2 if V_{IN2} is connected to SHOUT (0 otherwise).

DC1 = Duty cycle of channel 1 in steady state.

DC2 = Duty cycle of channel 2 in steady state.

η = Power conversion efficiency of Skyhook (typically 87%).

f = Switching frequency.

Skyhook Power Switch Current Overshoot: In order to avoid excessive current overshoot in the Skyhook power switch, $L_{OS(MIN)}$ should be:

$$L_{OS(MIN)} > \frac{V_{CC} \bullet t_D}{I_{OS}}$$

where:

V_{CC} = Input voltage of the Skyhook.

t_D = Skyhook fault current limit comparator delay (typically 50ns).

I_{OS} = The amount of overshoot current that can be tolerated (typically 100mA).

Current Rating: The maximum switch current limit for the Skyhook is 500mA. Choose an inductor that has a saturation current of 500mA or higher to avoid saturating the inductor.

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Compensation (Skyhook)

Like the primary channels, the Skyhook is internally compensated, and the loop stability is adjusted through the inductor and the output capacitor. In most applications, a 15µH Skyhook inductor such as Würth 744025150. and a 0.47µF Skyhook output capacitor (C3 in the Block Diagram) will give good stability. For high input voltage applications, more inductance is typically required to reduce the current overshoot.

A good technique to compensate the Skyhook regulator is to start with a 15µH Skyhook inductor and a 0.47µF output capacitor (C3 in the Block Diagram), and use the subsequent list to make additional adjustments if needed.

More output capacitance (C3 in the Block Diagram) can help with:

- Reducing the SHOUT overshoot and undershoot during primary channel(s) load steps.

Less output capacitance (C3 in the Block Diagram) can help with:

- Improving loop stability.
- Reducing peak inductor current during start-up.

More Skyhook inductance can help with:

- Reducing peak inductor current.

Less Skyhook inductance can help with:

- Improving loop stability when the SHOUT current load is consistently high (i.e., the primary channel(s) powered by SHOUT is switching every cycle).

Adding a resistor between SHOUT and C2, to introduce a few mA of constant load, can help with:

- Improving the loop stability, SHOUT undershoot and overshoot when the SHOUT current load is consistently very light (i.e., the primary channel(s) powered by SHOUT is not switching every cycle).

Thermal Considerations

For the LT8471 to deliver its full output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This can be accomplished by taking advantage of the thermal pad on the underside of the IC. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as possible.

Table 5. LT8471 Power Dissipation

DEFINITION OF VARIABLES	EQUATIONS	DESIGN EXAMPLE	VALUE
DC = Switch Duty Cycle	$DC = \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D - V_{CESAT}}$	$DC = \frac{12V - 5V + 0.45V}{12V + 0.45V - 0.21V}$	DC = 60.9%
I_{IN} = Average Switch Current η = Power Conversion Efficiency (typically 88% at high currents)	$I_{IN} = \frac{V_{OUT} \bullet I_{OUT}}{\eta \bullet V_{IN}}$	$I_{IN} = \frac{12V \bullet 0.67A}{0.88 \bullet 5V}$	I_{IN} = 1.85A
P_{SWDC} = Switch I^2R Loss (DC) R_{SW} = Switch Resistance (typically 200mΩ)	$P_{SWDC} = DC \bullet I_{IN}^2 \bullet R_{SW}$	$P_{SWDC} = 0.609 \bullet (1.85A)^2 \bullet 200m\Omega$	P_{SWDC} = 417mW
P_{SWAC} = Switch Dynamic Loss (AC)	$P_{SWAC} = 13ns \bullet I_{IN} \bullet V_{OUT} \bullet f_{OSC}$	$P_{SWAC} = (13ns) \bullet 1.85A \bullet 12V \bullet (1MHz)$	P_{SWAC} = 289mW
P_{BDC} = Base Drive Loss (DC)	$P_{BDC} = \frac{V_{IN} \bullet I_{IN} \bullet DC}{38}$	$P_{BDC} = \frac{5V \bullet 1.85A \bullet 0.609}{38}$	P_{BDC} = 148mW
P_{INP} = Input Power Loss	$P_{INP} = 2.5mA \bullet V_{IN}$	$P_{INP} = 2.5mA \bullet 5V$	P_{INP} = 12.5mW
	$P_{TOTAL} = (P_{SWDC} + P_{SWAC} + P_{BDC}) \bullet 2 + P_{INP}$	$P_{TOTAL} = (0.417 + 0.289 + 0.148) \bullet 2 + 0.0125$	P_{TOTAL} = 1.72W

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Power and Thermal Calculations

Power dissipation in the LT8471 chip comes from four primary sources: switch I^2R losses, switch dynamic losses, NPN base drive DC losses, and miscellaneous input current losses. These formulas assume continuous mode operation, so they should not be used for calculating thermal losses or efficiency in discontinuous mode or at light load currents.

The following example calculates the power dissipation in the LT8471 for a particular boost application on both CH1 and CH2 (V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.67A, f_{OSC} = 1MHz, V_D = 0.45V, V_{CESAT} = 0.21V).

To calculate die junction temperature, use the appropriate thermal resistance number and add in worst-case ambient temperature:

$$T_J = T_A + \theta_{JA} \bullet P_{TOTAL}$$

where T_J = Die Junction Temperature, T_A = Ambient Temperature, P_{TOTAL} is the final result from the calculations shown in Table 5, and θ_{JA} is the thermal resistance from the silicon junction to the ambient air.

The θ_{JA} value is 38°C/W for the 20-lead TSSOP package and 44°C/W for the 28-lead (4mm × 5mm) QFN package. In practice, lower θ_{JA} values can be realized if board layout is performed with appropriate grounding (accounting for heat sinking properties of the board) and other considerations listed in the Layout Guidelines section.

Thermal Lockout

A fault condition occurs when the die temperature exceeds 164°C (see Operation Section), and the part goes into thermal lockout. The fault condition ceases when the die temperature drops by ~1.5°C (nominal).

V_{IN} Ramp Rate

While initially powering a switching converter application, the V_{IN} ramp rate should be limited. High V_{IN} ramp rates can cause excessive inrush currents in the passive components of the converter. This can lead to current and/or voltage overstress and may damage the passive components or the chip. Ramp rates less than 500mV/µs, depending on component parameters, will generally prevent these issues. Also, be careful to avoid hot-plugging. Hot-plugging occurs when an active voltage supply is "instantly" connected or switched to the input of the converter. Hot-plugging results in very fast input ramp rates and is not recommended. Finally, for more information, refer to Linear application note AN88, which discusses voltage overstress that can occur when an inductive source impedance is hot-plugged to an input pin bypassed by ceramic capacitors.

Layout Guidelines

As with all high frequency switchers, when considering layout, care must be taken to achieve optimal electrical, thermal and noise performance. One will not get advertised performance with a careless layout. To prevent noise, both radiated and conducted, the high speed switching current paths must be kept as short as possible. For each channel, the high speed switching current flows in a loop through the following components:

- **Boost:** NPN power switch (C-E pins), external Schottky diode and output capacitor
- **Buck:** NPN power switch (C-E pins), external Schottky diode and input capacitor
- **1L Inverting:** NPN power switch (C-E pins), external Schottky diode, input capacitor and output capacitor

The area inside the loop formed by these components should be kept as small as possible. This is implemented in the suggested layouts shown in Figure 5, Figure 6 and Figure 7. Shortening the loop will also reduce the parasitic trace inductance. As the NPN switch turns off, the parasitic inductance can produce a flyback spike across the LT8471 switch. When operating at higher currents and output voltages, with poor layout, the spike can generate voltages across the switch that may exceed its absolute maximum rating. A ground plane should also be used under the switcher circuitry to prevent interplane coupling and overall noise. However, there should be no ground plane under the planes that are connected to

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the switching pins to keep the stray capacitance on the switching pins small.

Board layout also has a significant effect on thermal resistance. The exposed package ground pad is the copper plate that runs under the LT8471 die. This is a good thermal path for conducting heat out of the package. Soldering the pad onto the board reduces die temperature and increases the power capability of the LT8471. Provide as much copper area as possible around this pad. Adding multiple feedthroughs around the pad to the ground plane will also help. Figure 5, Figure 6, Figure 7 and Figure 8 show the recommended component placement for various DC/DC converter topologies.

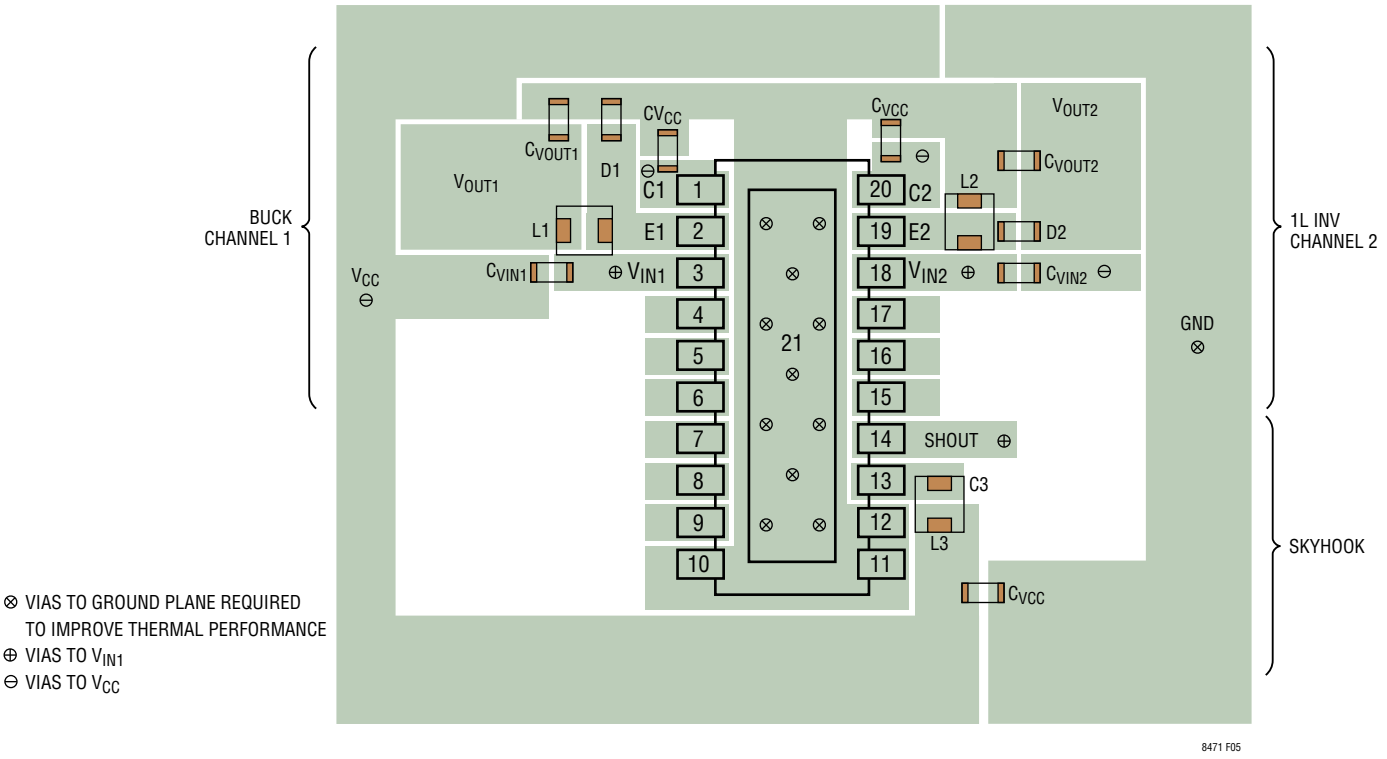

Figure 5. Suggested Component Placement for a Buck and Single-Inductor Inverting Converter (TSSOP Package)

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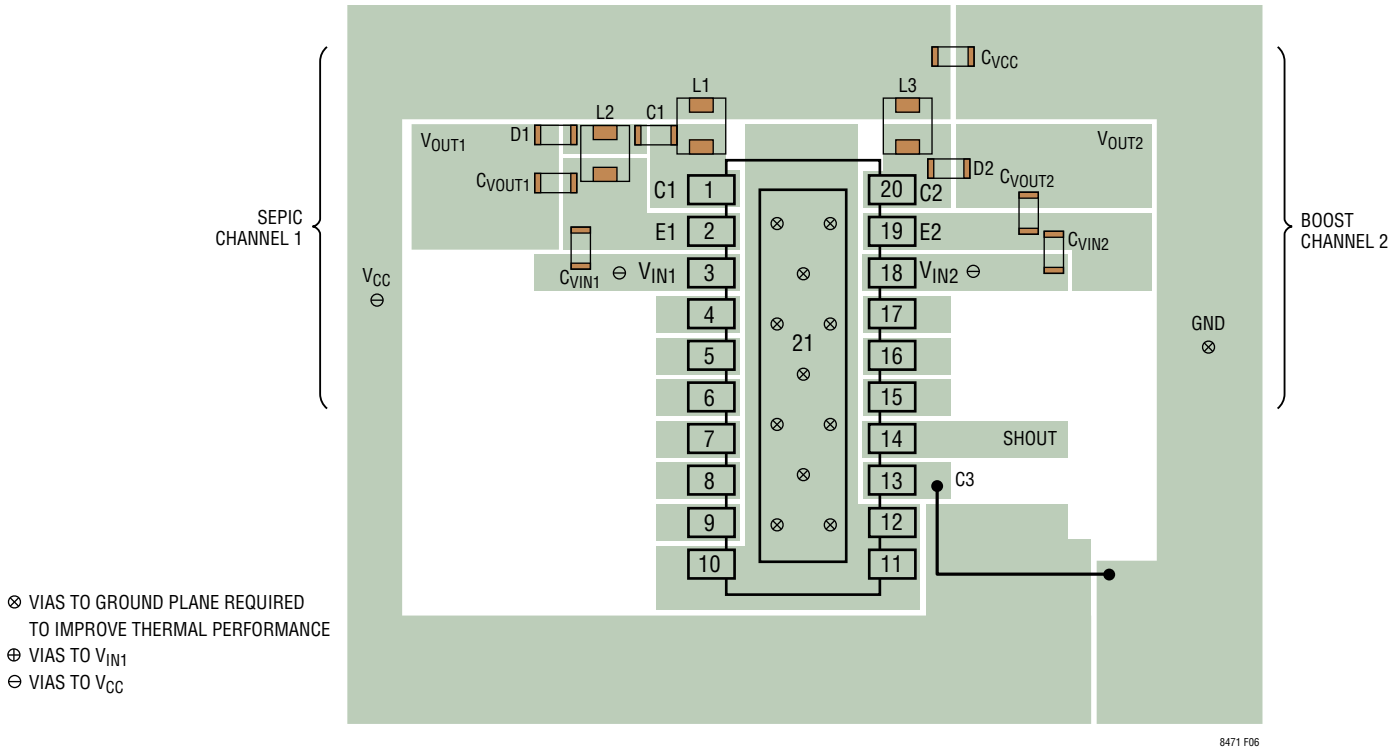

Figure 6. Suggested Component Placement for a SEPIC and Boost Converter (TSSOP Package)

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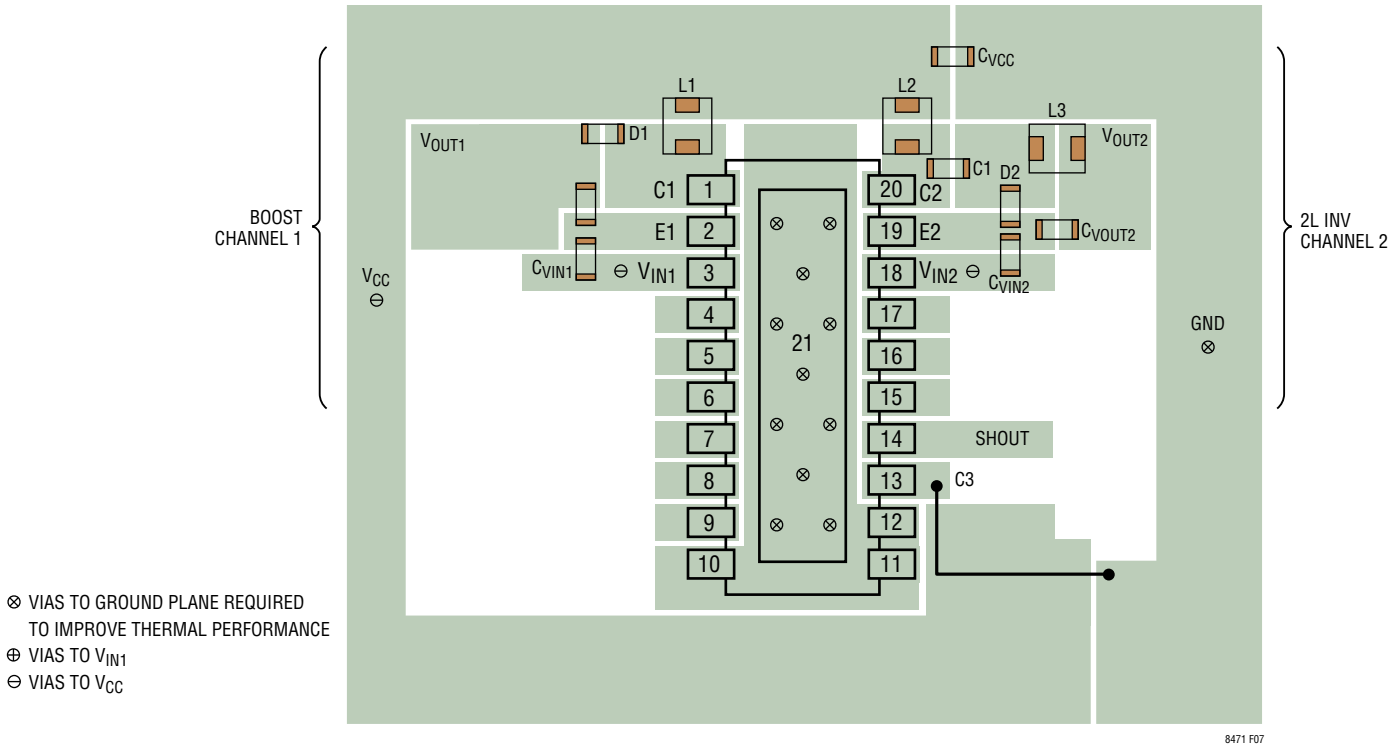

Figure 7. Suggested Component Placement for a Boost and Dual-Inductor Inverting Converter (TSSOP Package)

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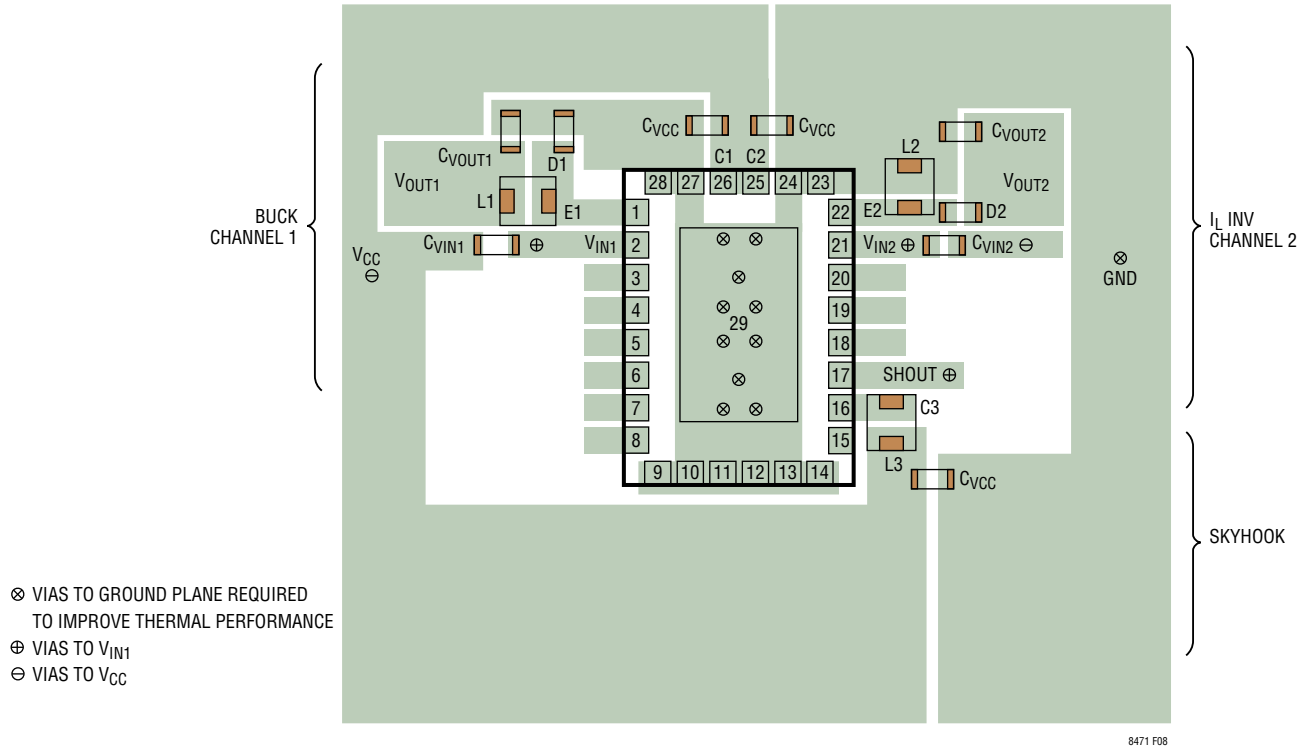

Figure 8. Suggested Component Placement for a Buck and Single-Inductor Inverting Converter (QFN Package)

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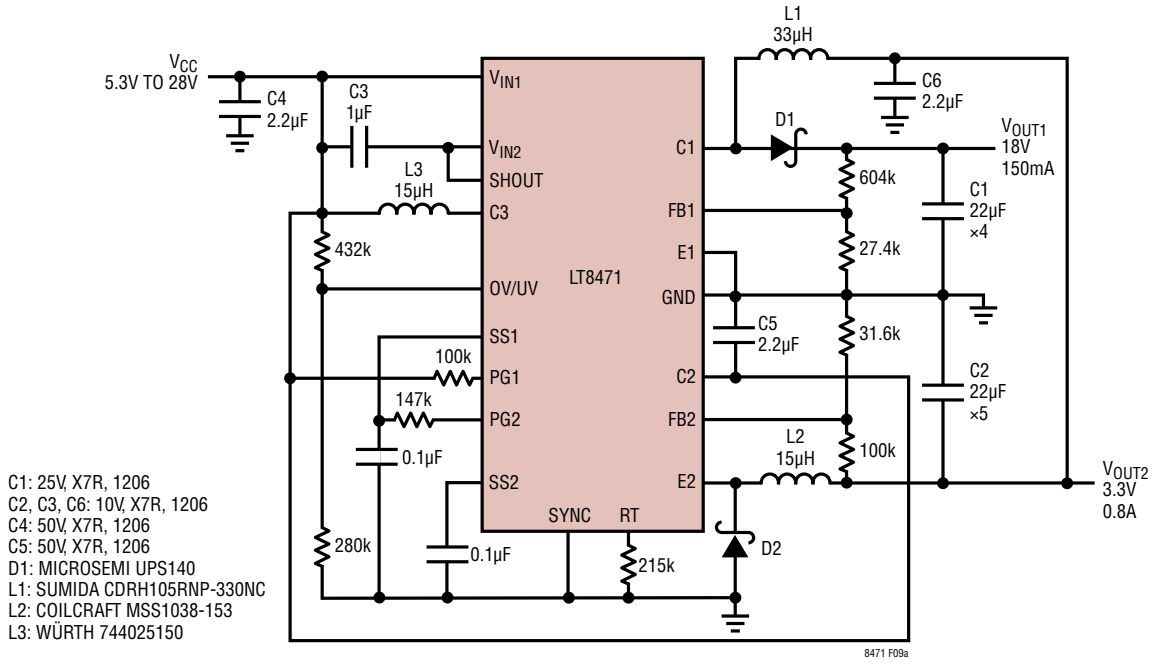

Figure 9a. Wide Input Range Buck Converter with 3.3V Output and Boost Converter with 18V Output at 400kHz

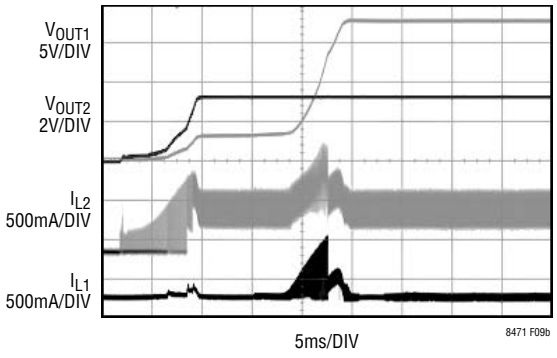

Figure 9b. Start-Up Waveforms

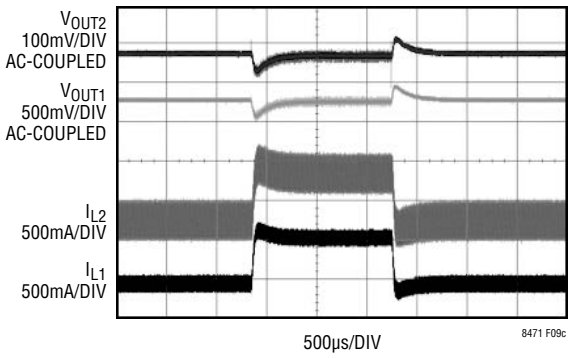

Figure 9c. Load Step on V_{OUT1} from 40mA to 135mA to 40mA

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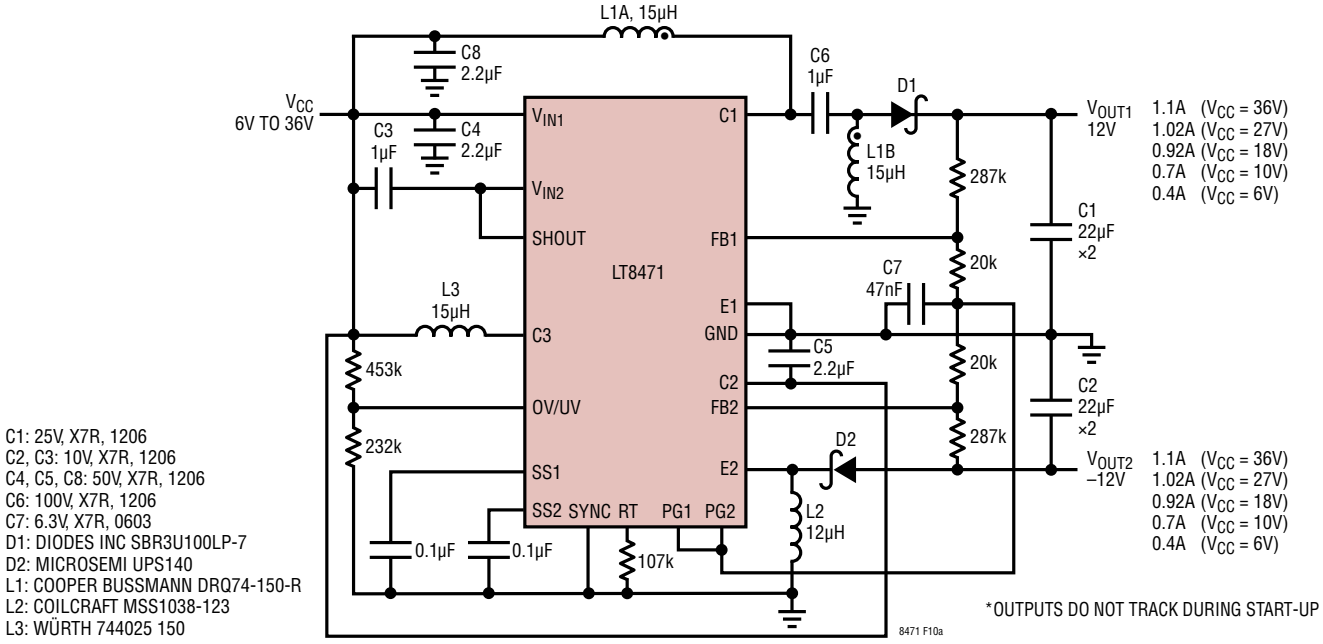


C1: 25V, X7R, 1206
C2, C3: 10V, X7R, 1206
C4, C5, C8: 50V, X7R, 1206
C6: 100V, X7R, 1206
C7: 6.3V, X7R, 0603
D1: DIODES INC SBR3U100LP-7
D2: MICROSEMI UPS140
L1: COOPER BUSSMANN DRQ74-150-R
L2: COILCRAFT MSS1038-123
L3: WÜRTH 744025 150

Figure 10a. Tracking* ±12V Supplies from 6V to 36V Input at 800kHz

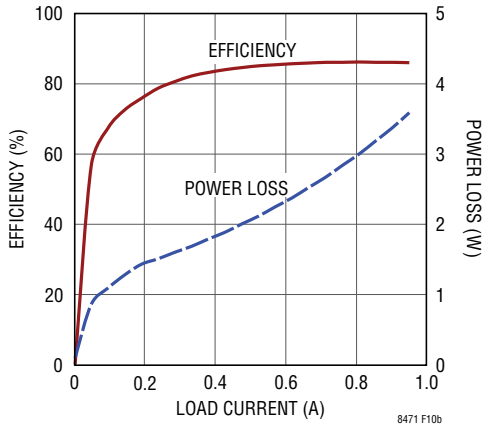


Figure 10b. Efficiency and Power Loss (V_{CC} = 18V, Load from V_{OUT1} to V_{OUT2})

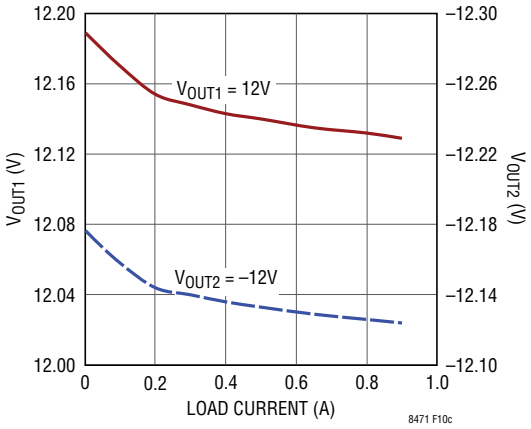


Figure 10c. 12V and –12V Outputs vs Load Current (V_{CC} = 18V, Load from V_{OUT1} to V_{OUT2})

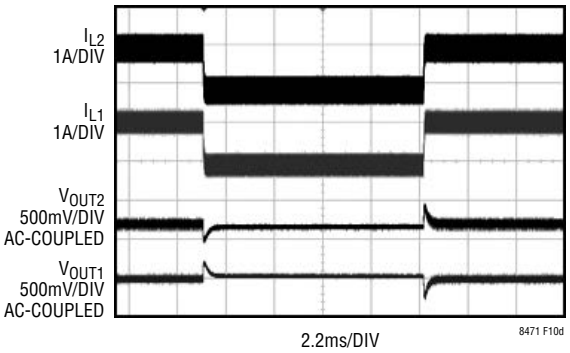


Figure 10d. Load Step Between V_{OUT1} and V_{OUT2} from 150mA to 780mA to 150mA (V_{CC} = 18V)

TYPICAL APPLICATIONS

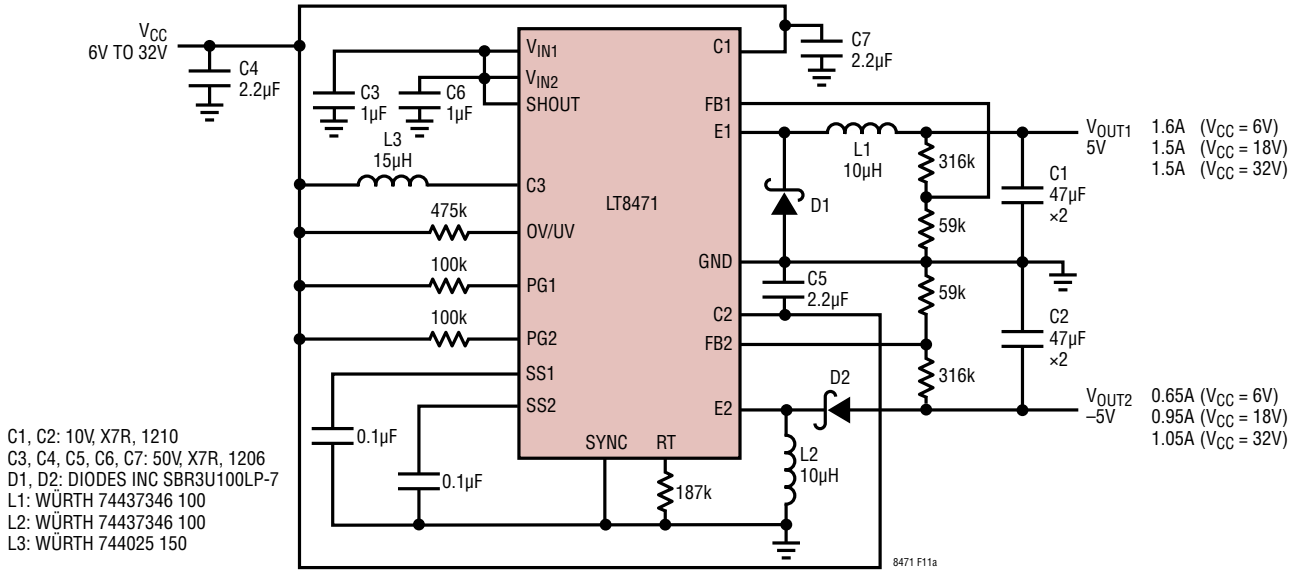


Figure 11a. Wide Input Range Converter with ±5V Output Voltages at 450kHz

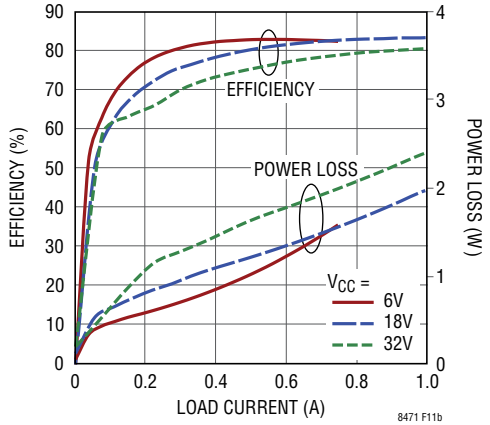
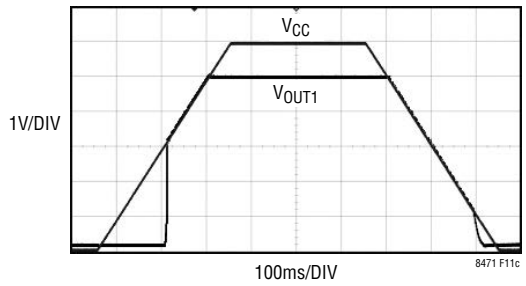
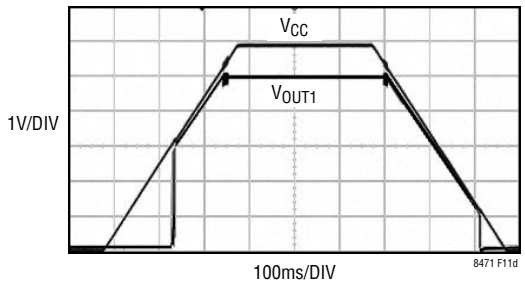


Figure 11b. Efficiency and Power Loss (Load from V_{OUT1} to V_{OUT2})



V_{CC} Is Ramped from 0V Up to 6V and Then Back Down to 0V. Channel 1 Output Voltage Is Loaded by a 100Ω Resistor

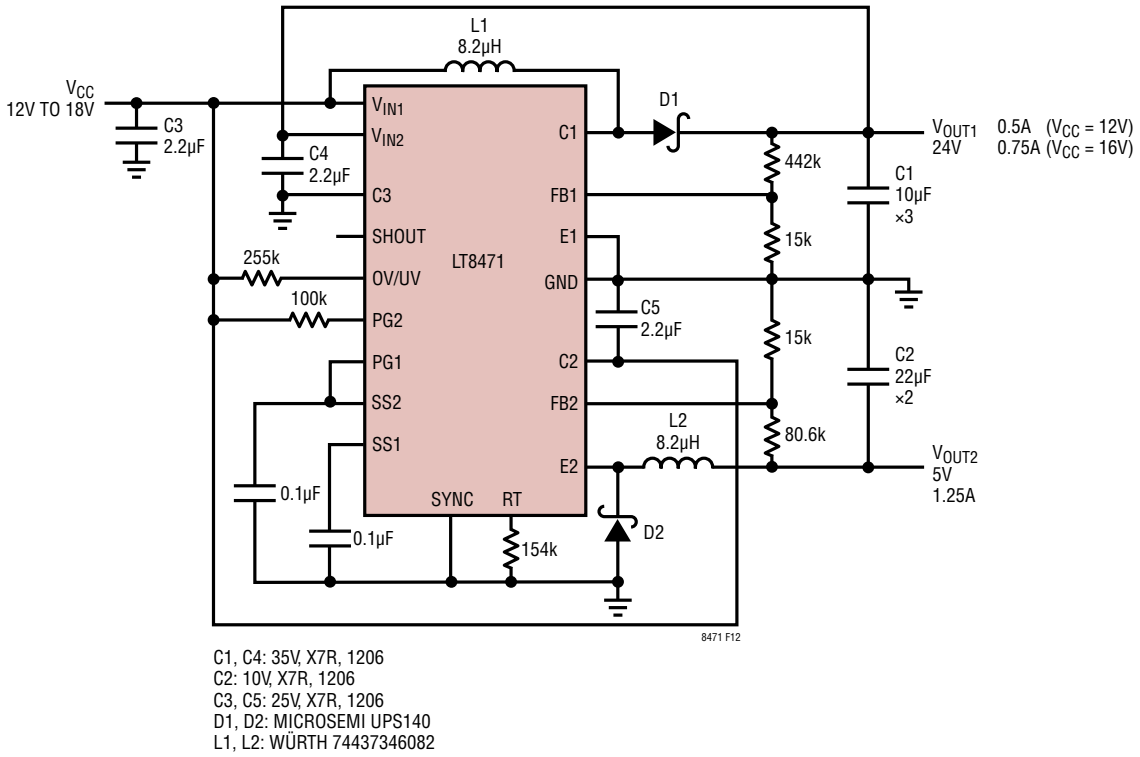
Figure 11c. Start-Up/Dropout Performance



V_{CC} Is Ramped from 0V Up to 6V and Then Back Down to 0V. Channel 1 Output Voltage Is Loaded by a 5Ω Resistor

Figure 11d. Start-Up/Dropout Performance

TYPICAL APPLICATIONS



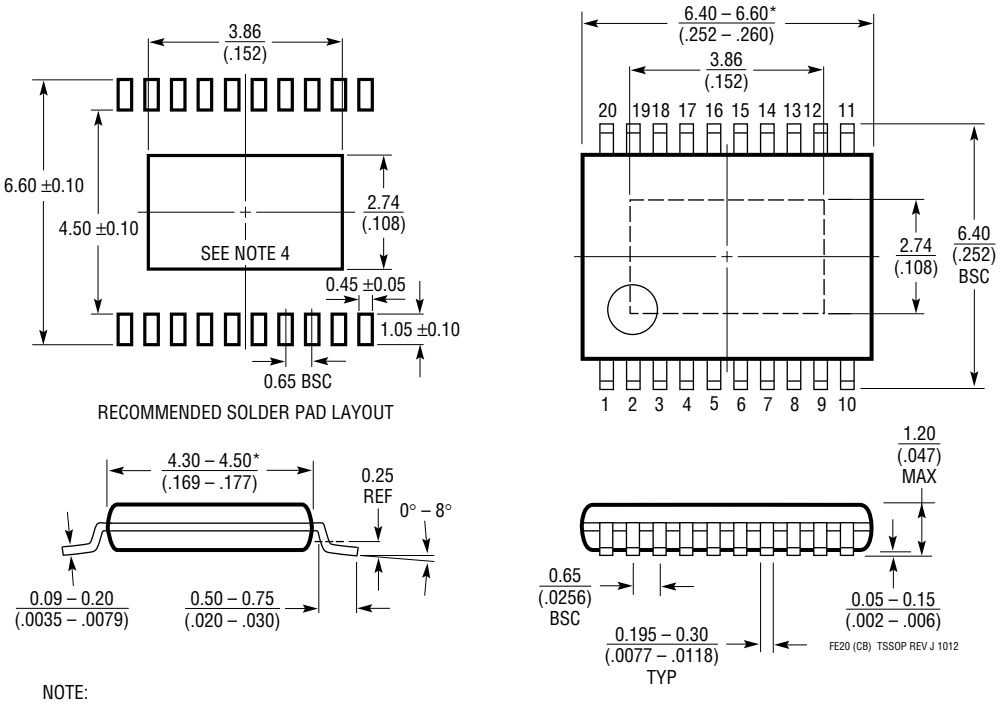
C1, C4: 35V, X7R, 1206
C2: 10V, X7R, 1206
C3, C5: 25V, X7R, 1206
D1, D2: MICROSEMI UPS140
L1, L2: WÜRTH 74437346082

Figure 12. Boost Converter with 24V Output and Buck Converter with 5V Output at 550kHz

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev J)
Exposed Pad Variation CB



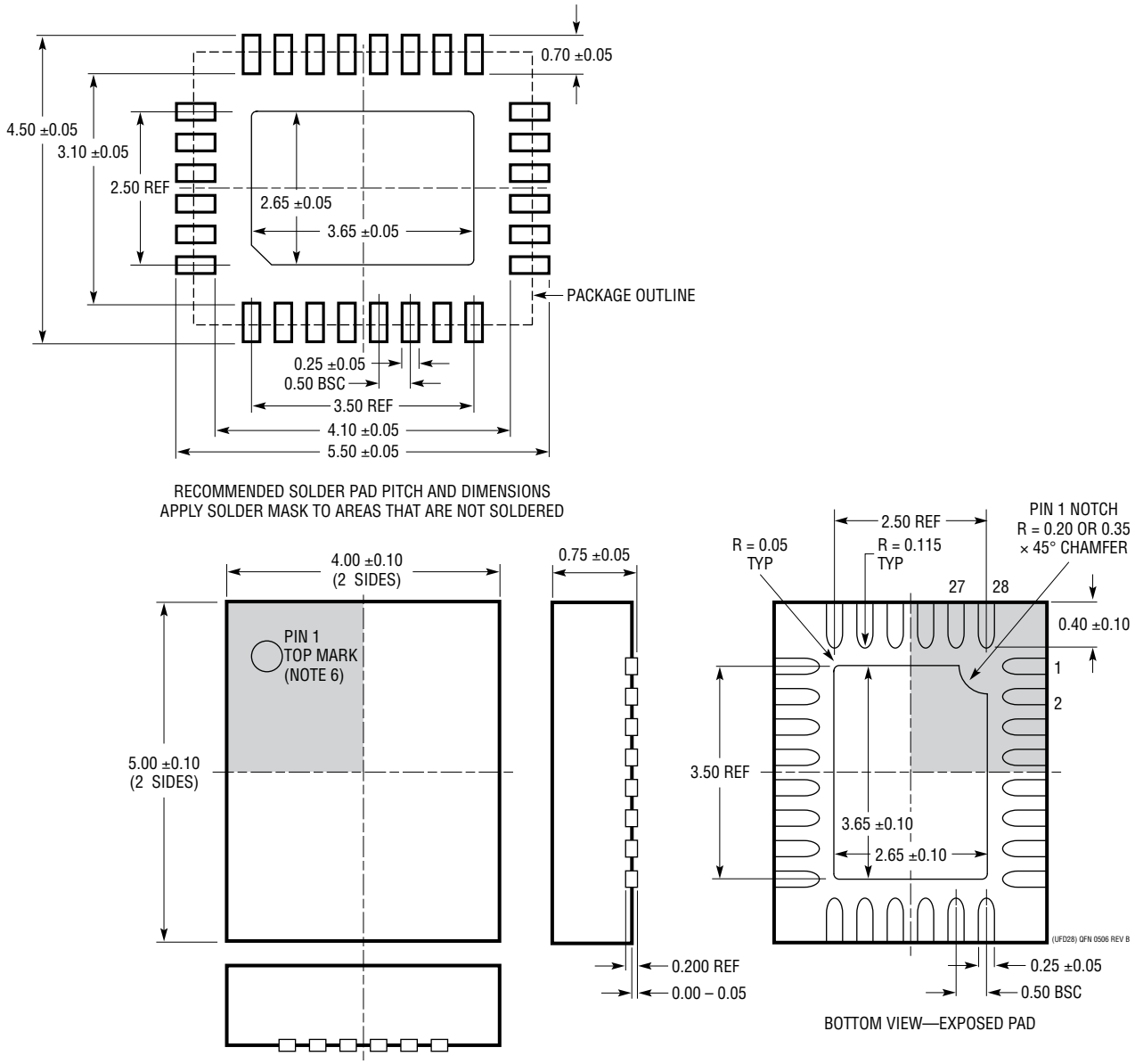
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



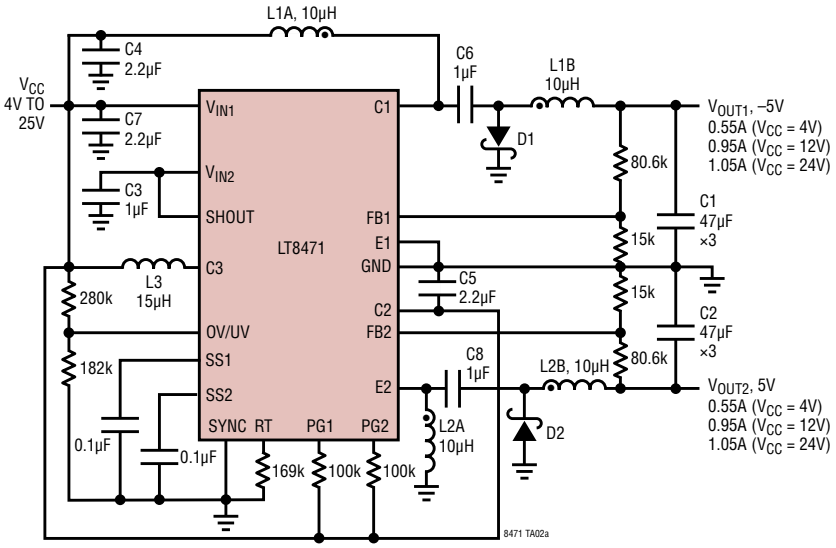
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/14	Clarified Applications Information Clarified Typical Applications	14 28, 29, 30, 31, 34
B	08/14	Clarified Operation Paragraph	9
		Clarified Applications Information 2nd Paragraph	10
		Clarified Typical Application	34
C	05/15	Added H-Grade Option	2, 3, 4
D	09/15	Added QFN Package Option	1, 2
		Added Zeta Configuration in Skyhook Channel Description	9
		Clarified Voltages to 1.4V	12
		Clarified Figure to 9A on Start-Up Sequencing Description	14
		Clarified Figure to 11A on Start-Up Sequencing Description	20
		Clarified Figure to 9A on Capacitor and Diode Selection Description	21
		Added QFN θ_{JA}	24
		Clarified Figure 5 (for TSSOP Package) added Reference to Figure 8	25
		Clarified Figure 5 (for TSSOP Package)	26
		Clarified Figure 5 (for TSSOP Package)	27
		Added Figure 8	28
		Relabeled Figures to 9A, 9B, 9C	29
		Relabeled Figures to 10A, 10B, 10C, 10D	30
		Relabeled Figures to 11A, 11B, 11C, 11D	31
		Relabeled Figures to 12	32
		Added QFN Package Drawing	34
		Relocated TSSOP Package Drawing	33
		Was Page 34-Now Page 36	36

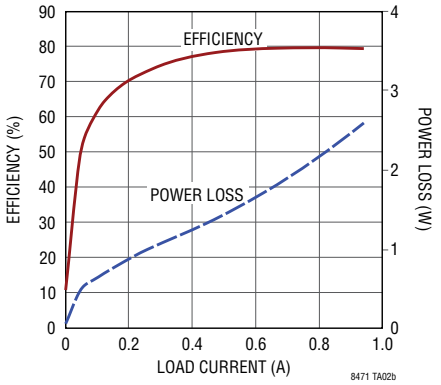
TYPICAL APPLICATION

500kHz ZETA and 2L Inverting Converters Generates ±5V Outputs with Low Output Ripple

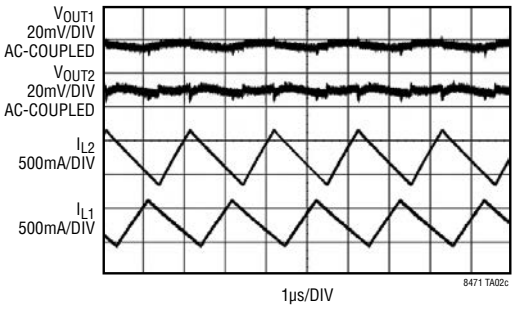


C1, C2: 10V, X7R, 1210
C3, C4, C5, C7: 35V, X7R, 1206
C6, C8: 50V, X7R, 1206
D1, D2: MICROSEMI UPS140
L1, L2: COOPER BUSSMANN DRQ74-100-R
L3: WÜRTH 744025 150

Efficiency and Power Loss V_{CC} = 12V, with Load Current from V_{OUT2} to V_{OUT1}



Output Voltage Ripple in CCM, V_{CC} = 10V



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8610/LT8611	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA and Input/Output Current Limit/Monitor (LT8611 Only)	V_{IN}: 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} <1µA, MSOP-16E and 3mm × 5mm QFN-24 Packages
LT8610A/LT8610AB	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN}: 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} <1µA, MSOP-16E and 3mm × 5mm QFN-24 Package
LT8582	40V, Dual 3A, 2.5MHz High Efficiency Boost Converter	V_{IN}: 2.5V to 22V, 40V_{MAX}, $V_{OUT(MAX)}$ = ±40V, I_Q = 2.8µA, I_{SD} <1µA, 7mm × 4mm DFN-24 Package
LT3581	40V, 3.3A, 2.5MHz High Efficiency Boost Converter	V_{IN}: 2.5V to 22V, 40V_{MAX}, $V_{OUT(MAX)}$ = ±40V, I_Q = 1mA, I_{SD} <1µA, 4mm × 3mm DFN-14 and MSOP-16E Packages
LT8582	40V, Dual 3A Boost, Inverter, SEPIC, 2.5MHz High Efficiency Boost Converter	V_{IN}: 2.5V to 22V, 40V_{MAX}, $V_{OUT(MAX)}$ = ±40V, I_Q = 2.1mA, I_{SD} <1µA, 7mm × 4mm DFN-24 Package
LT3579/LT3579-1	40V, 3.3A Boost, Inverter, SEPIC, 2.5MHz High Efficiency Boost Converter	V_{IN}: 2.5V to 22V, 40V_{MAX}, $V_{OUT(MAX)}$ = ±40V, I_Q = 1mA, I_{SD} <1µA, 4mm × 5mm QFN-20 and TSSOP-20E Packages
LT3471	40V Dual 1.3A Boost, Inverter, 1.2MHz High Efficiency Boost Converter	V_{IN}: 2.4V to 16V, 40V_{MAX}, $V_{OUT(MAX)}$ = ±40V, I_Q = 2.4mA, I_{SD} <1µA, 3mm × 3mm DFN Package

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear.com/8471
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