LINEAR TECHNOLOGY

1.6V, 1µA Precision Rail-to-Rail Input and Output Op Amps

FEATURES

- **Wide Supply Range: 1.6V to 16V**
- **Low Supply Current: 1µA/Amplifier Max**
- **Low Input Bias Current: 90pA Max**
- Low Input Offset Voltage: 500µV Max
- Low Input Offset Voltage Drift: 2µV/°C
- CMRR: 100dB
- PSRR: 95dB
- A_{VOL} Driving 20kΩ Load: 100,000 Min
- Capacitive Load Handling: 500pF
- Specified from –40°C to 125°C
- Available in Tiny 2mm × 2mm DFN and Low Profile (1mm) ThinSOT™ Packages

APPLICATIONS

- Portable Gas Monitors
- Battery- or Solar-Powered Systems
- Low Voltage Signal Processing
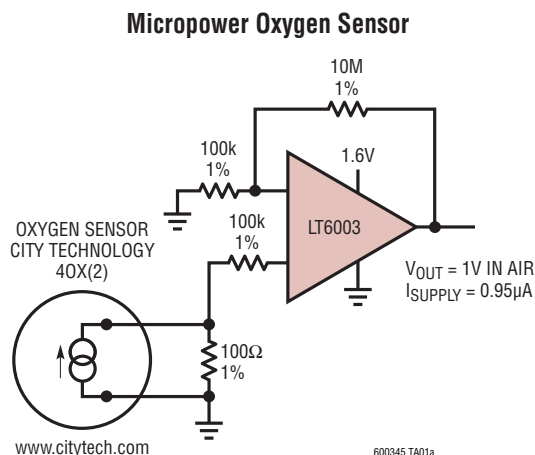- Micropower Active Filters

DESCRIPTION

The LT6003CDC#PBF are single/dual/quad op amps designed to maximize battery life and performance for portable applications. These amplifiers operate on supplies as low as 1.6V and are fully specified and guaranteed over temperature on 1.8V, 5V and ±8V supplies while only drawing 1µA maximum quiescent current.

The ultralow supply current and low operating voltage are combined with excellent amplifier specifications; input offset voltage of 500µV maximum with a typical drift of only 2µV/°C, input bias current of 90pA maximum, open loop gain of 100,000 and the ability to drive 500pF capacitive loads, making the LT6003/LT6004/LT6005 amplifiers ideal when excellent performance is required in battery powered applications.
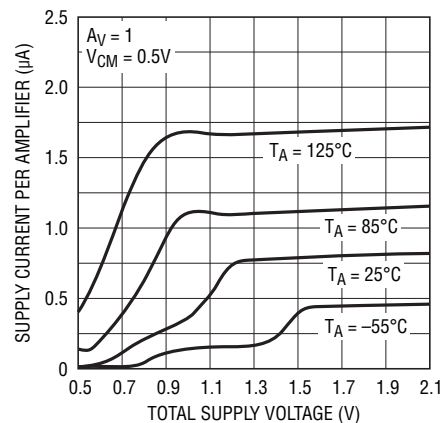
The single LT6003 is available in the 5-pin TSOT-23 and tiny 2mm × 2mm DFN packages. The dual LT6004 is available in the 8-pin MSOP and 3mm × 3mm DFN packages. The quad LT6005 is available in the 16-pin SSOP and 5mm × 3mm DFN packages. These devices are specified over the commercial, industrial and automotive temperature ranges.

TYPICAL APPLICATION

Micropower Oxygen Sensor

10M 1%
100k 1%
1.6V
LT6003
OXYGEN SENSOR CITY TECHNOLOGY 4OX(2)
100k 1%
100Ω 1%
V_{OUT} = 1V IN AIR
I_{SUPPLY} = 0.95µA
www.citytech.com
600345 TA01a

Start-Up Characteristics
Supply Current vs Supply Voltage

A_V = 1
V_{CM} = 0.5V
T_A = 125°C
T_A = 85°C
T_A = 25°C
T_A = –55°C
SUPPLY CURRENT PER AMPLIFIER (µA)
TOTAL SUPPLY VOLTAGE (V)
600345 TA01b

600345fd

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V$^+$ to V$^-$) 18V
Differential Input Voltage...18V
Input Voltage Below V$^-$ 9V
Input Current..10mA
Output Short Circuit Duration (Note 2)............. Indefinite
Operating Temperature Range (Note 3)
   LT6003C, LT6004C, LT6005C .... −40°C to 85°C
   LT6003I, LT6004I, LT6005I.................. −40°C to 85°C
   LT6003H, LT6004H, LT6005H............. −40°C to 125°C

Specified Temperature Range (Note 4)
   LT6003C, LT6004C, LT6005C .... 0°C to 70°C
   LT6003I, LT6004I, LT6005I.................. −40°C to 85°C
   LT6003H, LT6004H, LT6005H............. −40°C to 125°C
Junction Temperature
   DFN Packages...................................... 125°C
   All Other Packages.............................. 150°C
Storage Temperature Range
   DFN Packages................................. −65°C to 125°C
   All Other Packages........................... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)
   TSOT, MSOP, SSOP Packages .... 300°C

PIN CONFIGURATION

LT6003

TOP VIEW

+IN [1]
−IN [2]
OUT [3]
V$^+$ [4]
[5]

DC PACKAGE
4-LEAD (2mm × 2mm) PLASTIC DFN

T$_{JMAX}$ = 125°C, θ$_{JA}$ = 102°C/W (NOTE 2)
EXPOSED PAD (PIN 5) IS V$^-$,
MUST BE SOLDERED TO PCB

LT6003

TOP VIEW

OUT 1
V$^-$ 2
+IN 3
5 V$^+$
4 −IN

S5 PACKAGE
5-LEAD PLASTIC TSOT-23

T$_{JMAX}$ = 150°C, θ$_{JA}$ = 250°C/W

LT6004

TOP VIEW

OUT A [1]
−IN A [2]
+IN A [3]
V$^-$ [4]
[9]
[8] V$^+$
[7] OUT B
[6] −IN B
[5] +IN B

DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T$_{JMAX}$ = 125°C, θ$_{JA}$ = 160°C/W (NOTE 2)
EXPOSED PAD (PIN 9) CONNECTED TO V$^-$
(PCB CONNECTION OPTIONAL)

LT6004

TOP VIEW

OUT A 1
−IN A 2
+IN A 3
V$^-$ 4
8 V$^+$
7 OUT B
6 −IN B
5 +IN B

MS8 PACKAGE
8-LEAD PLASTIC MSOP

T$_{JMAX}$ = 150°C, θ$_{JA}$ = 250°C/W

LT6005

TOP VIEW

OUT A [1]
−IN A [2]
+IN A [3]
V$^+$ [4]
+IN B [5]
−IN B [6]
OUT B [7]
NC [8]
[17]
[16] OUT D
[15] −IN D
[14] +IN D
[13] V$^-$
[12] +IN C
[11] −IN C
[10] OUT C
[9] NC

DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN

T$_{JMAX}$ = 125°C, θ$_{JA}$ = 160°C/W (NOTE 2)
EXPOSED PAD (PIN 17) CONNECTED TO V$^-$,
(PCB CONNECTION OPTIONAL)

LT6005

TOP VIEW

OUT A [1]
−IN A [2]
+IN A [3]
V$^+$ [4]
+IN B [5]
−IN B [6]
OUT B [7]
NC [8]
[16] OUT D
[15] −IN D
[14] +IN D
[13] V$^-$
[12] +IN C
[11] −IN C
[10] OUT C
[9] NC

GN PACKAGE
16-LEAD PLASTIC SSOP

T$_{JMAX}$ = 150°C, θ$_{JA}$ = 135°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6003CDC#PBF	LT6003CDC#TRPBF	LCKF	4-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6003IDC#PBF	LT6003IDC#TRPBF	LCKF	4-Lead (2mm × 2mm) Plastic DFN	−40°C to 85°C
LT6003HDC#PBF	LT6003HDC#TRPBF	LCKF	4-Lead (2mm × 2mm) Plastic DFN	−40°C to 125°C
LT6003CS5#PBF	LT6003CS5#TRPBF	LTCKG	5-Lead Plastic TSOT-23	0°C to 70°C
LT6003IS5#PBF	LT6003IS5#TRPBF	LTCKG	5-Lead Plastic TSOT-23	−40°C to 85°C
LT6003HS5#PBF	LT6003HS5#TRPBF	LTCKG	5-Lead Plastic TSOT-23	−40°C to 125°C
LT6004CDD#PBF	LT6004CDD#TRPBF	LCCB	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT6004IDD#PBF	LT6004IDD#TRPBF	LCCB	8-Lead (3mm × 3mm) Plastic DFN	−40°C to 85°C
LT6004HDD#PBF	LT6004HDD#TRPBF	LCCB	8-Lead (3mm × 3mm) Plastic DFN	−40°C to 125°C
LT6004CMS8#PBF	LT6004CMS8#TRPBF	LTCBZ	8-Lead Plastic MSOP	0°C to 70°C
LT6004IMS8#PBF	LT6004IMS8#TRPBF	LTCBZ	8-Lead Plastic MSOP	−40°C to 85°C
LT6004HMS8#PBF	LT6004HMS8#TRPBF	LTCBZ	8-Lead Plastic MSOP	−40°C to 125°C
LT6005CDHC#PBF	LT6005CDHC#TRPBF	6005	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LT6005IDHC#PBF	LT6005IDHC#TRPBF	6005	16-Lead (5mm × 3mm) Plastic DFN	−40°C to 85°C
LT6005HDHC#PBF	LT6005HDHC#TRPBF	6005	16-Lead (5mm × 3mm) Plastic DFN	−40°C to 125°C
LT6005CGN#PBF	LT6005CGN#TRPBF	6005	16-Lead Plastic SSOP	0°C to 70°C
LT6005IGN#PBF	LT6005IGN#TRPBF	6005I	16-Lead Plastic SSOP	−40°C to 85°C
LT6005HGN#PBF	LT6005HGN#TRPBF	6005H	16-Lead Plastic SSOP	−40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS
(LT6003C/I, LT6004C/I, LT6005C/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_S = 1.8V$, 0V, $V_{CM} = 0.5V$; $V_S = 5V$, 0V, $V_{CM} = 2.5V$, V_{OUT} = half supply, R_L to ground, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6003S5, LT6004MS8			175	500	µV
		$0°C ≤ T_A ≤ 70°C$	●			725	µV
		$−40°C ≤ T_A ≤ 85°C$	●			950	µV
		LT6005GN			190	650	µV
		$0°C ≤ T_A ≤ 70°C$	●			925	µV
		$−40°C ≤ T_A ≤ 85°C$	●			1.15	mV
		LT6004DD, LT6005DHC			290	850	µV
		$0°C ≤ T_A ≤ 70°C$	●			1.15	mV
		$−40°C ≤ T_A ≤ 85°C$	●			1.4	mV
		LT6003DC			290	950	µV
		$0°C ≤ T_A ≤ 70°C$	●			1.3	mV
		$−40°C ≤ T_A ≤ 85°C$	●			1.6	mV
$ΔV_{OS}/ΔT$	Input Offset Voltage Drift (Note 5)	S5, MS8, GN	●		2	5	µV/°C
		DC, DD, DHC	●		2	7	µV/°C

ELECTRICAL CHARACTERISTICS

(LT6003C/I, LT6004C/I, LT6005C/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_S = 1.8V$, 0V, $V_{CM} = 0.5V$; $V_S = 5V$, 0V, $V_{CM} = 2.5V$, V_{OUT} = half supply, R_L to ground, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_B	Input Bias Current (Note 7)	$V_{CM} = 0.3V$, $0°C \leq T_A \leq 70°C$	●		5	90	pA
		$V_{CM} = V^+ - 0.3V$, $0°C \leq T_A \leq 70°C$	●		40	140	pA
		$V_{CM} = 0.3V$, $-40°C \leq T_A \leq 85°C$	●		5	120	pA
		$V_{CM} = V^+ - 0.3V$, $-40°C \leq T_A \leq 85°C$	●		40	170	pA
		$V_{CM} = 0V$	●		0.13	1.4	nA
I_{OS}	Input Offset Current (Note 7)	$V_{CM} = 0.3V$	●		5	80	pA
		$V_{CM} = V^+ - 0.3V$	●		7	80	pA
		$V_{CM} = 0V$	●		5	100	pA
	Input Noise Voltage	0.1Hz to 10Hz			3		μV_{P-P}
e_n	Input Noise Voltage Density	f = 100Hz			325		nV/$\sqrt{Hz}$
i_n	Input Noise Current Density	f = 100Hz			12		fA/$\sqrt{Hz}$
R_{IN}	Input Resistance	Differential			10		GΩ
		Common Mode			2000		GΩ
C_{IN}	Input Capacitance				6		pF
CMRR	Common Mode Rejection Ratio (Note 7)	$V_S = 1.8V$					
		V_{CM} = 0V to 0.7V	●	73	100		dB
		V_{CM} = 0V to 1.8V, S5, MS8, GN	●	63	80		dB
		V_{CM} = 0V to 1.8V, DC, DD, DHC	●	60	78		dB
		$V_S = 5V$					
		V_{CM} = 0V to 3.9V	●	88	115		dB
		V_{CM} = 0V to 5V, S5, MS8, GN	●	72	90		dB
		V_{CM} = 0V to 5V, DC, DD, DHC	●	69	86		dB
	Input Offset Voltage Shift (Note 7)	V_{CM} = 0V to $V^+ - 1.1V$	●		7	155	μV
		V_{CM} = 0V to V^+, S5, MS8, GN	●		0.16	1.3	mV
		V_{CM} = 0V to V^+, DC, DD, DHC	●		0.23	1.8	mV
	Input Voltage Range	Guaranteed by CMRR	●	0		V^+	V
PSRR	Power Supply Rejection Ratio	V_S = 1.6V to 6V, V_{CM} = 0.5V, $0°C \leq T_A \leq 70°C$	●	80	95		dB
		V_S = 1.7V to 6V, V_{CM} = 0.5V, $-40°C \leq T_A \leq 85°C$	●	78	95		dB
	Minimum Supply Voltage	Guaranteed by PSRR, $0°C \leq T_A \leq 70°C$	●	1.6			V
		$-40°C \leq T_A \leq 85°C$	●	1.7			V
A_{VOL}	Large Signal Voltage Gain (Note 7)	$V_S = 1.8V$		25	150		V/mV
		$R_L = 20k\Omega$, V_{OUT} = 0.25V to 1.25V	●	15			V/mV
		$V_S = 5V$		100	500		V/mV
		$R_L = 20k\Omega$, V_{OUT} = 0.25V to 4.25V	●	60			V/mV
V_{OL}	Output Swing Low (Notes 6, 8)	No Load	●		15	50	mV
		I_{SINK} = 100μA	●		110	240	mV
V_{OH}	Output Swing High (Notes 6, 9)	No Load	●		45	100	mV
		I_{SOURCE} = 100μA	●		200	350	mV
I_{SC}	Short Circuit Current (Note 8)	Short to GND		2	5		mA
		$0°C \leq T_A \leq 70°C$	●	1.5			mA
		$-40°C \leq T_A \leq 85°C$	●	0.5			mA
		Short to V^+		2	7		mA
		$0°C \leq T_A \leq 70°C$	●	1.5			mA
		$-40°C \leq T_A \leq 85°C$	●	0.5			mA
I_S	Supply Current per Amplifier	$V_S = 1.8V$			0.85	1	μA
		$0°C \leq T_A \leq 70°C$	●			1.4	μA
		$-40°C \leq T_A \leq 85°C$	●			1.6	μA
		$V_S = 5V$			1	1.2	μA
		$0°C \leq T_A \leq 70°C$	●			1.6	μA
		$-40°C \leq T_A \leq 85°C$	●			1.9	μA

600345fd

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LINEAR TECHNOLOGY

ELECTRICAL CHARACTERISTICS

(LT6003C/I, LT6004C/I, LT6005C/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 1.8V, 0V, V_{CM} = 0.5V; V_S = 5V, 0V, V_{CM} = 2.5V, V_{OUT} = half supply, R_L to ground, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GBW	Gain Bandwidth Product	f = 100Hz			2		kHz
SR	Slew Rate (Note 11)	A_V = −1, R_F = R_G = 1MΩ		0.55	0.8		V/ms
		0°C ≤ T_A ≤ 70°C	●	0.4			V/ms
		−40°C ≤ T_A ≤ 85°C	●	0.2			V/ms
FPBW	Full Power Bandwidth	V_{OUT} = 1.5V_{P-P} (Note 10)			170		Hz

(LT6003H, LT6004H, LT6005H) The ● denotes the specifications which apply over the full specified temperature range of −40°C ≤ T_A ≤ 125°C. V_S = 1.8V, 0V, V_{CM} = 0.5V; V_S = 5V, 0V, V_{CM} = 2.5V, V_{OUT} = half supply, R_L to ground, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6003S5, LT6004MS8	●			1.5	mV
		LT6005GN	●			1.7	mV
		LT6004DD, LT6005DHC	●			1.9	mV
		LT6003DC				2.1	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 5)	S5, MS8, GN	●		2	6	µV/°C
		DC, DD, DHC	●		3	8	µV/°C
I_B	Input Bias Current (Note 7)	LT6003, V_{CM} = 0.3V, V^+ − 0.3V	●			6	nA
		LT6004, LT6005, V_{CM} = 0.3V, V^+ − 0.3V	●			12	nA
I_{OS}	Input Offset Current (Note 7)	LT6003, V_{CM} = 0.3V, V^+ − 0.3V	●			2	nA
		LT6004, LT6005, V_{CM} = 0.3V, V^+ − 0.3V	●			4	nA
CMRR	Common Mode Rejection Ratio (Note 7)	V_S = 1.8V					
		V_{CM} = 0.3V to 0.7V	●	67			dB
		V_{CM} = 0.3V to 1.5V, S5, MS8, GN	●	57			dB
		V_{CM} = 0.3V to 1.5V, DC, DD, DHC	●	55			dB
		V_S = 5V					
		V_{CM} = 0.3V to 3.9V	●	86			dB
		V_{CM} = 0.3V to 4.7V, S5, MS8, GN	●	68			dB
		V_{CM} = 0.3V to 4.7V, DC, DD, DHC	●	66			dB
	Input Offset Voltage Shift (Note 7)	V_{CM} = 0.3V to V^+ − 1.1V	●			180	µV
		V_{CM} = 0.3V to V^+ − 0.3V, S5, MS8, GN	●			1.7	mV
		V_{CM} = 0.3V to V^+ − 0.3V, DC, DD, DHC	●			2.2	mV
	Input Voltage Range	Guaranteed by CMRR	●	0.3		V^+ − 0.3V	V
PSRR	Power Supply Rejection Ratio	V_S = 1.7V to 6V, V_{CM} = 0.5V	●	76			dB
	Minimum Supply	Guaranteed by PSRR	●	1.7			V
A_{VOL}	Large Signal Voltage Gain (Note 7)	V_S = 1.8V, R_L = 20kΩ, V_{OUT} = 0.4V to 1.25V	●	4			V/mV
		V_S = 5V, R_L = 20kΩ, V_{OUT} = 0.4V to 4.25V	●	20			V/mV
V_{OL}	Output Swing Low (Notes 6, 8)	No Load	●			60	mV
		I_{SINK} = 100µA	●			275	mV
V_{OH}	Output Swing High (Notes 6, 9)	No Load	●			120	mV
		I_{SOURCE} = 100µA	●			400	mV
I_{SC}	Short Circuit Current (Note 8)	Short to GND	●	0.5			mA
		Short to V^+	●	0.5			mA
I_S	Supply Current per Amplifier	V_S = 1.8V	●			2.2	µA
		V_S = 5V	●			2.5	µA
SR	Slew Rate (Note 11)	A_V = −1, R_F = R_G = 1MΩ	●	0.2			V/ms

ELECTRICAL CHARACTERISTICS

(LT6003C/I, LT6004C/I, LT6005C/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_S = ±8V$, $V_{CM} = V_{OUT}$ = half supply, R_L to ground, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6003S5, LT6004MS8 $0°C ≤ T_A ≤ 70°C$ $−40°C ≤ T_A ≤ 85°C$	 ● ●		185	600 825 1.05	µV µV mV
		LT6005GN $0°C ≤ T_A ≤ 70°C$ $−40°C ≤ T_A ≤ 85°C$	 ● ●		200	750 1.05 1.25	µV mV mV
		LT6004DD, LT6005DHC $0°C ≤ T_A ≤ 70°C$ $−40°C ≤ T_A ≤ 85°C$	 ● ●		300	950 1.25 1.5	µV mV mV
		LT6003DC $0°C ≤ T_A ≤ 70°C$ $−40°C ≤ T_A ≤ 85°C$	 ● ●		0.3	1.05 1.4 1.65	mV mV mV
$ΔV_{OS}/ΔT$	Input Offset Voltage Drift (Note 5)	S5, MS8, GN DC, DD, DHC	● ●		2 2	5 7	µV/°C µV/°C
I_B	Input Bias Current	$0°C ≤ T_A ≤ 70°C$ $−40°C ≤ T_A ≤ 85°C$	● ●		7 7	100 150	pA pA
I_{OS}	Input Offset Current		●		7	90	pA
	Input Noise Voltage	0.1Hz to 10Hz			3		µV$_{P-P}$
e_n	Input Noise Voltage Density	f = 100Hz			325		nV/√Hz
i_n	Input Noise Current Density	f = 100Hz			12		fA/√Hz
R_{IN}	Input Resistance	Differential Common Mode			10 2000		GΩ GΩ
C_{IN}	Input Capacitance				6		pF
CMRR	Common Mode Rejection Ratio	$V_{CM} = −8V$ to 6.9V $V_{CM} = −8V$ to 8V, S5, MS8, GN $V_{CM} = −8V$ to 8V, DC, DD, DHC	● ● ●	92 82 78	120 100 96		dB dB dB
	Input Offset Voltage Shift	$V_{CM} = −8V$ to 6.9V $V_{CM} = −8V$ to 8V, S5, MS8, GN $V_{CM} = −8V$ to 8V, DC, DD, DHC	● ● ●		15 0.16 0.25	375 1.3 2	µV mV mV
	Input Voltage Range	Guaranteed by CMRR	●	−8		8	V
PSRR	Power Supply Rejection Ratio	$V_S = ±1.1V$ to ±8V	●	86	105		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 100kΩ$, $V_{OUT} = −7.3V$ to 7.3V			350		V/mV
V_{OL}	Output Swing Low (Notes 6, 8)	No Load $I_{SINK} = 100µA$	● ●		10 105	50 240	mV mV
V_{OH}	Output Swing High (Notes 6, 9)	No Load $I_{SOURCE} = 100µA$	● ●		50 195	120 350	mV mV
I_{SC}	Short Circuit Current	Short to GND $0°C ≤ T_A ≤ 70°C$ $−40°C ≤ T_A ≤ 85°C$	 ● ●	4 3 1	9		mA mA mA
I_S	Supply Current per Amplifier	 $0°C ≤ T_A ≤ 70°C$ $−40°C ≤ T_A ≤ 85°C$	 ● ●		1.25	1.5 1.9 2.2	µA µA µA
GBW	Gain Bandwidth Product	f = 100Hz			3		kHz
SR	Slew Rate (Note 11)	$A_V = −1$, $R_F = R_G = 1MΩ$ $0°C ≤ T_A ≤ 70°C$ $−40°C ≤ T_A ≤ 85°C$	 ● ●	0.55 0.4 0.2	1.3		V/ms V/ms V/ms
FPBW	Full Power Bandwidth	$V_{OUT} = 14V_{P-P}$ (Note 10)			30		Hz

LINEAR TECHNOLOGY

ELECTRICAL CHARACTERISTICS

(LT6003H, LT6004H, LT6005H) The ● denotes the specifications which apply over the full specified temperature range of −40°C ≤ T_A ≤ 125°C. V_S = ±8V, V_{CM} = V_{OUT} = half supply, R_L to ground, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6003S5, LT6004MS8 LT6005GN LT6004DD, LT6005DHC LT6003DC	● ● ● ●			1.6 1.8 2 2.2	mV mV mV mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 5)	S5, MS8, GN DC, DD, DHC	● ●		2 3	6 8	µV/°C µV/°C
I_B	Input Bias Current	LT6003 LT6004, LT6005	● ●			6 12	nA nA
I_{OS}	Input Offset Current	LT6003 LT6004, LT6005	● ●			2 4	nA nA
CMRR	Common Mode Rejection Ratio	V_{CM} = −7.7V to 6.9V V_{CM} = −7.7V to 7.7V, S5, MS8, GN V_{CM} = −7.7V to 7.7V, DC, DD, DHC	● ● ●	90 78 76			dB dB dB
	Input Offset Voltage Shift	V_{CM} = −7.7V to 6.9V V_{CM} = −7.7V to 7.7V, S5, MS8, GN V_{CM} = −7.7V to 7.7V, DC, DD, DHC	● ● ●			460 1.9 2.5	µV mV mV
	Input Voltage Range	Guaranteed by CMRR	●	−7.7		7.7	V
PSRR	Power Supply Rejection Ratio	V_S = ±1.1V to ±8V	●	84			dB
V_{OL}	Output Swing Low (Notes 6, 8)	No Load I_{SINK} = 100µA	● ●			60 275	mV mV
V_{OH}	Output Swing High (Note 6)	No Load I_{SOURCE} = 100µA	● ●			140 400	mV mV
I_{SC}	Short Circuit Current	Short to GND	●	1			mA
I_S	Supply Current per Amplifier		●			3	µA
SR	Slew Rate (Note 11)	A_V = −1, R_F = R_G = 1MΩ	●	0.2			V/ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. The θ_JA specified for the DC, DD and DHC packages is with minimal PCB heat spreading metal. Using expanded metal area on all layers of a board reduces this value.

Note 3: The LT6003C/LT6004C/LT6005C and LT6003I/LT6004I/LT6005I are guaranteed functional over the temperature range of −40°C to 85°C. The LT6003H/LT6004H/LT6005H are guaranteed functional over the operating temperature range of −40°C to 125°C.

Note 4: The LT6003C/LT6004C/LT6005C are guaranteed to meet specified performance from 0°C to 70°C. The LT6003C/LT6004C/LT6005C are designed, characterized and expected to meet specified performance from

−40°C to 85°C but are not tested or QA sampled at these temperatures. The LT6003I/LT6004I/LT6005I are guaranteed to meet specified performance from −40°C to 85°C. The LT6003H/LT6004H/LT6005H are guaranteed to meet specified performance from −40°C to 125°C.

Note 5: This parameter is not 100% tested.

Note 6: Output voltage swings are measured between the output and power supply rails.

Note 7: Limits are guaranteed by correlation to V_S = 5V tests.

Note 8: Limits are guaranteed by correlation to V_S = 1.8V tests

Note 9: Limits are guaranteed by correlation to V_S = ±8V tests

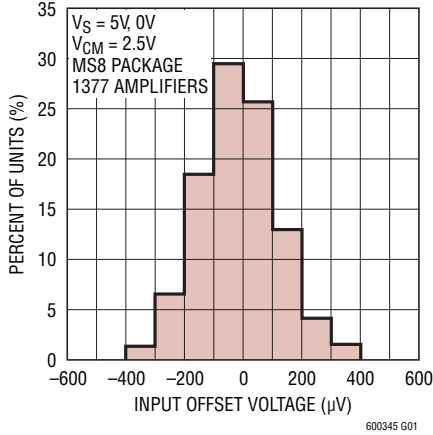**Note 10:** Full-power bandwidth is calculated from the slew rate:
FPBW = SR/πV_{P-P}.

Note 11: Slew rate measured at V_S = 1.8V, V_{OUT} = 0.4V to 1.4V is used to guarantee by correlation the slew rate at V_S = 5V, V_{OUT} = 1V to 4V and the slew rate at V_S = ±8V, V_{OUT} = −5V to 5V.
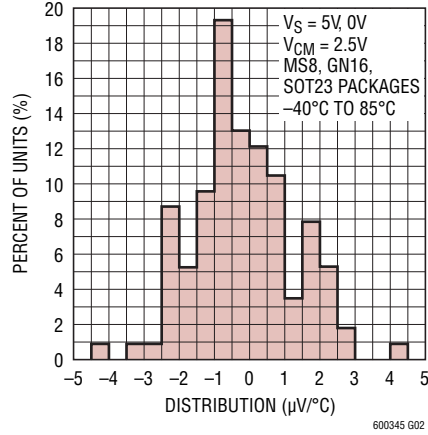
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OS} Distribution

$V_S = 5V, 0V$
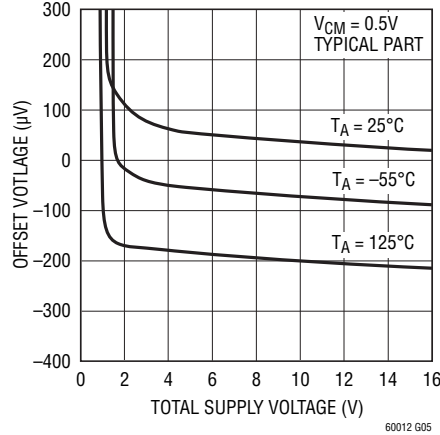$V_{CM} = 2.5V$
MS8 PACKAGE
1377 AMPLIFIERS

PERCENT OF UNITS (%)
INPUT OFFSET VOLTAGE (µV)
600345 G01

TC V_{OS} Distribution

$V_S = 5V, 0V$
$V_{CM} = 2.5V$
MS8, GN16,
SOT23 PACKAGES
−40°C TO 85°C

PERCENT OF UNITS (%)
DISTRIBUTION (µV/°C)
600345 G02

Supply Current vs Supply Voltage

$V_{CM} = 0.5V$
$T_A = 125°C$
$T_A = 85°C$
$T_A = 25°C$
$T_A = -55°C$

SUPPLY CURRENT PER AMPLIFIER (µA)
SUPPLY VOLTAGE (V)
600345 G03
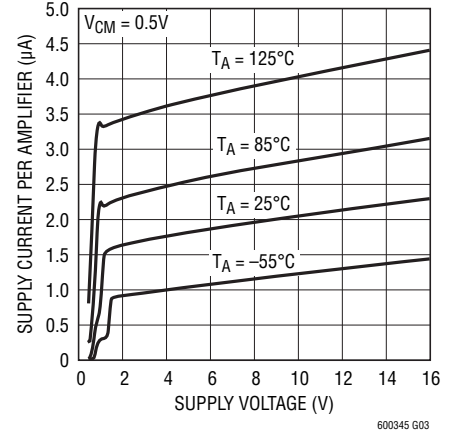
Change in Input Offset Voltage vs Total Supply Voltage

$T_A = -55°C$
$T_A = 25°C$
$T_A = 125°C$

CHANGE IN OFFSET VOLTAGE (µV)
TOTAL SUPPLY VOLTAGE (V)
600345 G04

Input Offset Voltage vs Total Supply Voltage

$V_{CM} = 0.5V$
TYPICAL PART
$T_A = 25°C$
$T_A = -55°C$
$T_A = 125°C$

OFFSET VOTLAGE (µV)
TOTAL SUPPLY VOLTAGE (V)
60012 G05
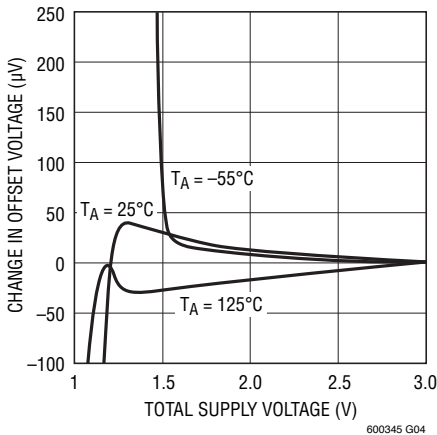
Input Offset Voltage vs Input Common Mode Voltage

$T_A = 25°C$
$T_A = -55°C$
$T_A = 125°C$
$V_S = 5V, 0V$
TYPICAL PART

INPUT OFFSET VOLTAGE (µV)
INPUT COMMON MODE VOLTAGE (V)
600345 G06
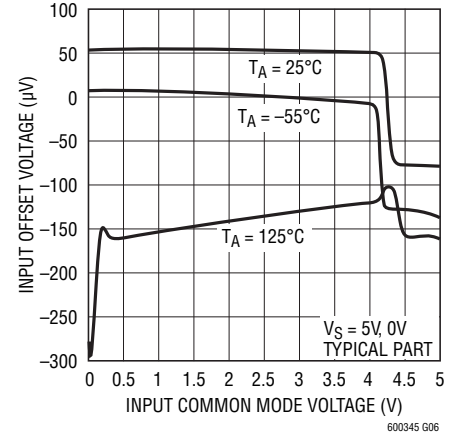
Input Bias Current vs Common Mode Voltage
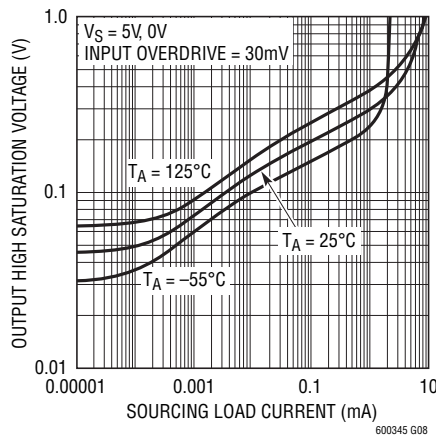
$V_S = 5V, 0V$
$T_A = 125°C$
$T_A = 85°C$
$T_A = -55°C$
$T_A = 25°C$

INPUT BIAS CURRENT (nA)
COMMON MODE VOLTAGE (V)
600345 G07

Output Saturation Voltage vs Load Current (Output High)

$V_S = 5V, 0V$
INPUT OVERDRIVE = 30mV
$T_A = 125°C$
$T_A = 25°C$
$T_A = -55°C$

OUTPUT HIGH SATURATION VOLTAGE (V)
SOURCING LOAD CURRENT (mA)
600345 G08

Output Saturation Voltage vs Load Current (Output Low)

$V_S = 5V, 0V$
INPUT OVERDRIVE = 30mV
$T_A = 125°C$
$T_A = -55°C$
$T_A = 25°C$

OUTPUT LOW SATURATION VOLTAGE (V)
SINKING LOAD CURRENT (mA)
600345 G09

600345fd

8

LINEAR
TECHNOLOGY
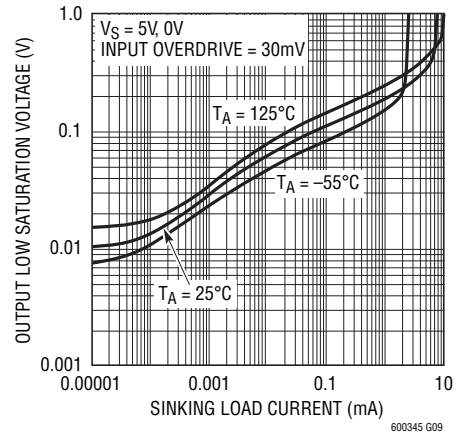
TYPICAL PERFORMANCE CHARACTERISTICS

Output Saturation Voltage vs Input Overdrive

$V_S = \pm 2.5V$
NO LOAD

OUTPUT HIGH

OUTPUT LOW

600345 G10
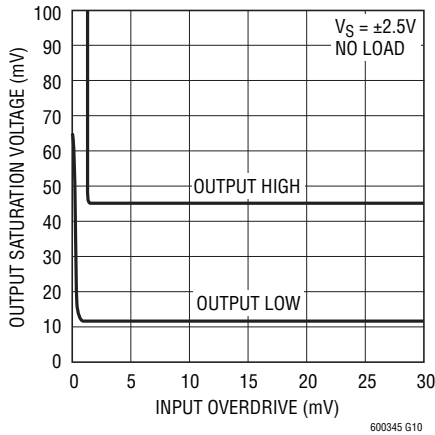
Output Short-Circuit Current vs Total Supply Voltage (Sourcing)

$V_{CM} = 0.5V$
OUTPUT SHORTED TO V^-

$T_A = 125°C$

$T_A = 25°C$

$T_A = -55°C$

600345 G11
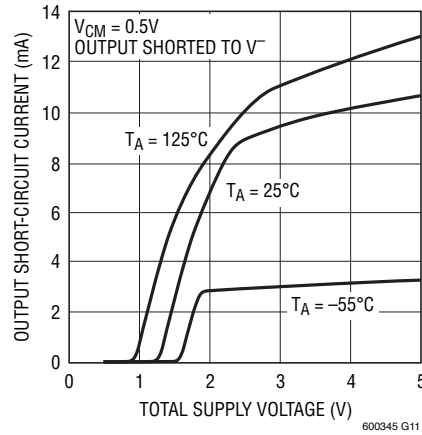
Output Short-Circuit Current vs Total Supply Voltage (Sinking)

$V_{CM} = 0.5V$
OUTPUT SHORTED TO V^+

$T_A = 125°C$

$T_A = 25°C$

$T_A = -55°C$

600345 G12
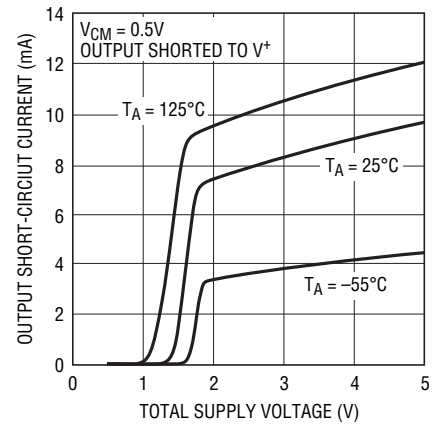
0.1Hz to 10Hz Voltage Noise

$V_S = \pm 2.5V$
$T_A = 25°C$

600345 G13
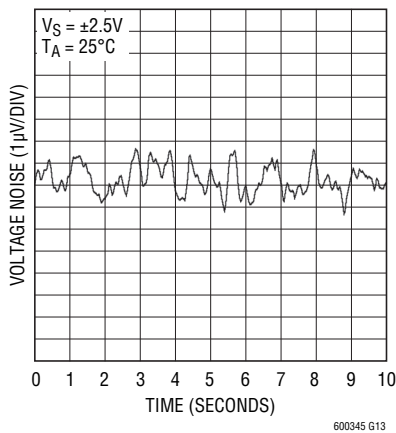
Voltage Noise vs Frequency

$V_S = 5V, 0V$
$T_A = 25°C$

$V_{CM} = 4.5V$

$V_{CM} = 2.5V$

600345 G14
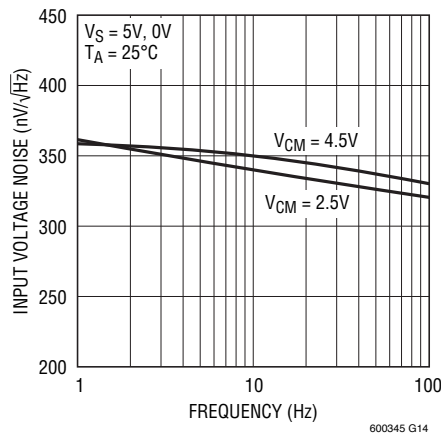
Current Noise vs Frequency

$V_S = 5V, 0V$
$T_A = 25°C$

$V_{CM} = 4.5V$

$V_{CM} = 2.5V$

600345 G15

Open-Loop Gain

$V_S = 1.8V, 0V$
$V_{CM} = 0.5V$
$T_A = 25°C$

$R_L = 1M$

$R_L = 100k$

$R_L = 20k$

600345 G16

Open-Loop Gain

$V_S = 5V, 0V$
$V_{CM} = 0.5V$
$T_A = 25°C$

$R_L = 100k$

$R_L = 1M$

$R_L = 20k$

600345 G17

Open-Loop Gain

$V_S = \pm 8V$
$T_A = 25°C$

$R_L = 20k$

$R_L = 100k$

$R_L = 1M$

600345 G18

600345fd
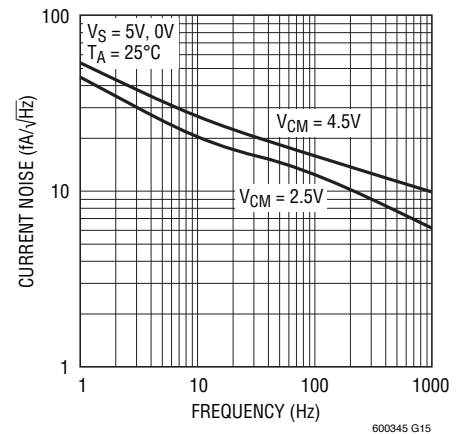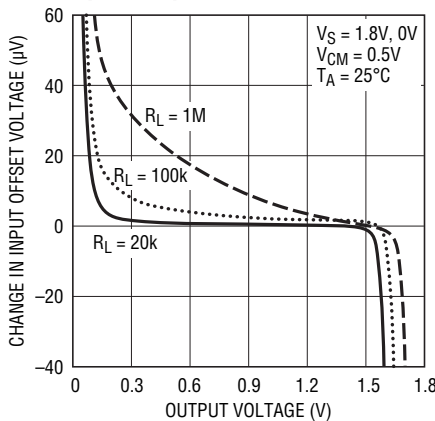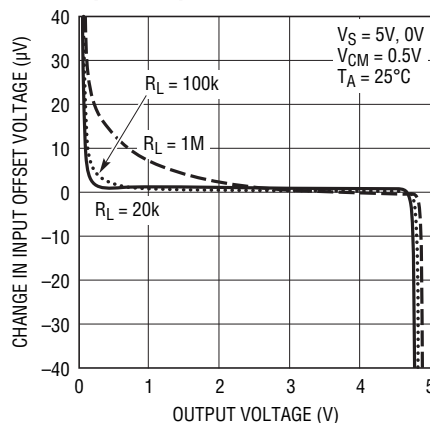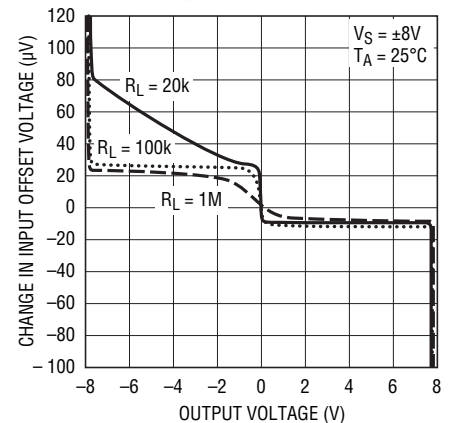
TYPICAL PERFORMANCE CHARACTERISTICS

Gain Bandwidth and Phase Margin vs Total Supply Voltage

600345 G19
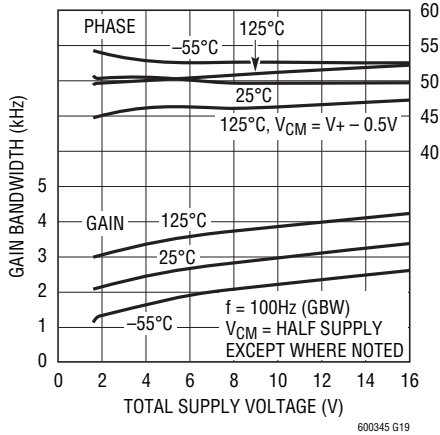
Slew Rate vs Temperature

600345 G20
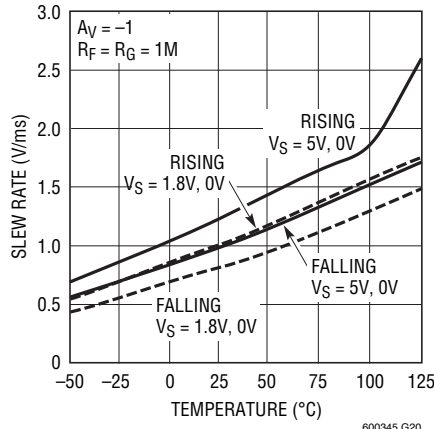
Gain and Phase vs Frequency

600345 G21
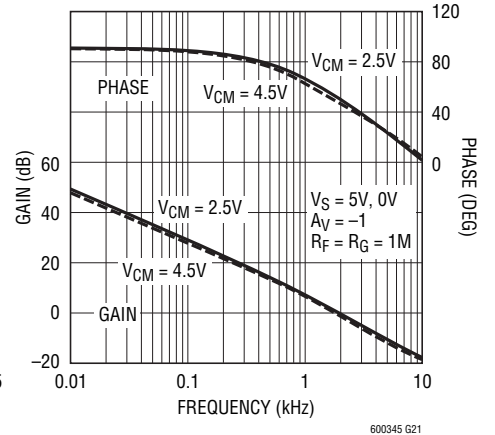
Capacitive Load Handling Overshoot vs Capacitive Load
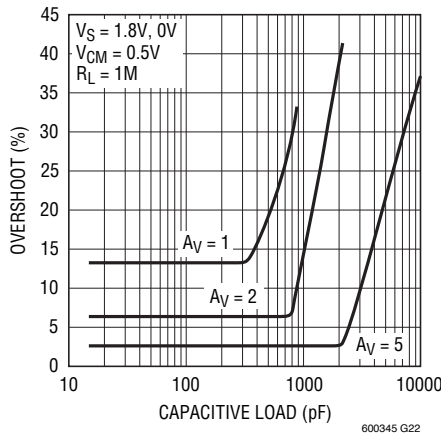
600345 G22

Common Mode Rejection Ratio vs Frequency

600345 G23

Power Supply Rejection Ratio vs Frequency

600345 G24
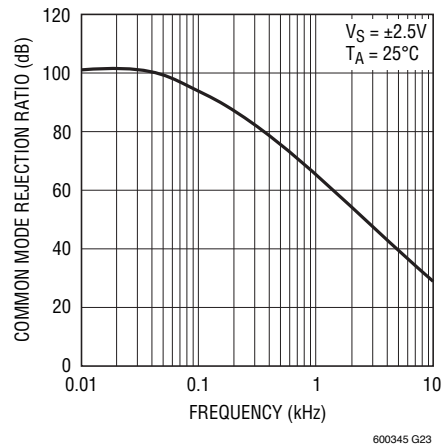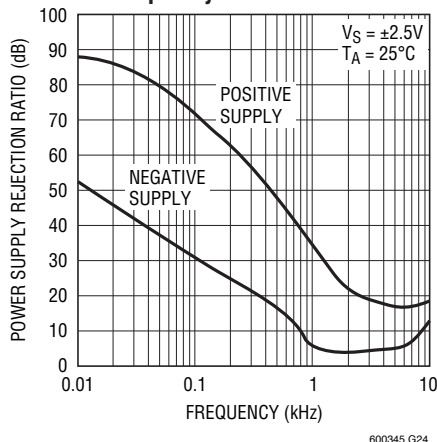
Output Impedance vs Frequency

600345 G25

600345fd

10
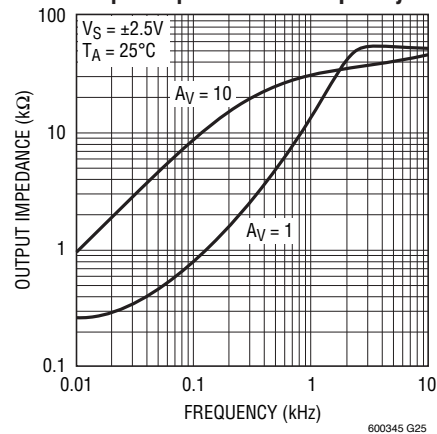
TYPICAL PERFORMANCE CHARACTERISTICS

Large-Signal Response

$A_V = 1$
$V_S = 5V, 0V$
$C_L = 100pF$
$R_L = 100k$

1ms/DIV

600345 G26

Large-Signal Response

$A_V = 1$
$V_S = 1.8V, 0V$
$C_L = 100pF$
$R_L = 100k$

1ms/DIV

600345 G2

Small-Signal Response

$A_V = 1$
$V_S = \pm2.5V$
$C_L = 50pF$
$R_L = 1M$

200µs/DIV

600345 G28
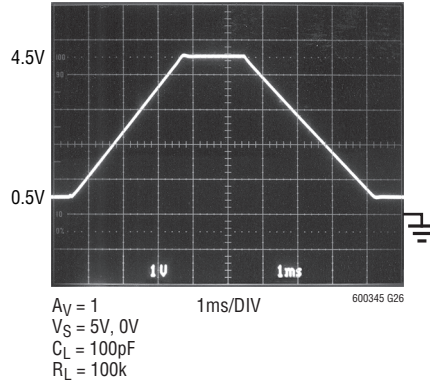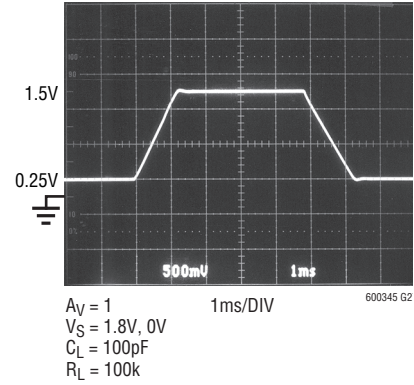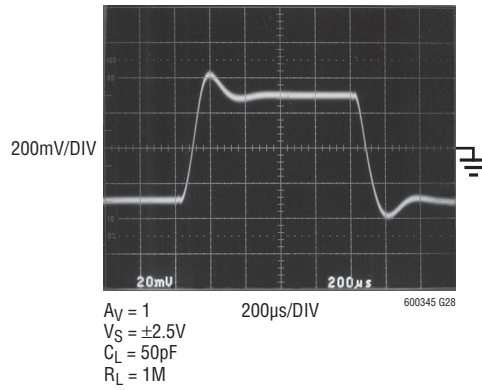
Output Saturation Recovery

$A_V = -1$
$V_S = \pm2.5V$
$R_F = R_G = 1M$

5ms/DIV

600345 G29
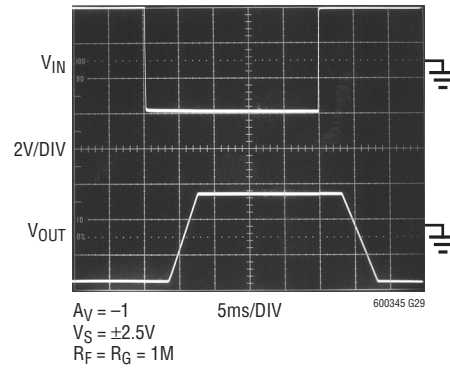
SIMPLIFIED SCHEMATIC

Figure 1

APPLICATIONS INFORMATION

Supply Voltage

The positive supply of the LT6003/LT6004/LT6005 should be bypassed with a small capacitor (about 0.01µF) within an inch of the pin. When driving heavy loads, an additional 4.7µF electrolytic capacitor should be used. When using split supplies, the same is true for the negative supply pin.

Rail-to-Rail Characteristics

The LT6003/LT6004/LT6005 are fully functional for an input signal range from the negative supply to the positive supply. Figure 1 shows a simplified schematic of the amplifier. The input stage consists of two differential amplifiers, a PNP stage Q3/Q6 and an NPN stage Q4/ Q5 that are active over different ranges of the input common mode voltage. The PNP stage is active for common mode voltages, V_{CM}, between the negative supply to approximately 0.9V below the positive supply. As V_{CM} moves closer towards the positive supply, the transistor Q7 will steer Q2's tail current to the current mirror Q8/Q9, activating the NPN differential pair. The PNP pair becomes inactive for the rest of the input common mode voltage range up to the positive supply.

The second stage is a folded cascode and current mirror that converts the input stage differential signals into a single ended output. Capacitor C1 reduces the unity cross frequency and improves the frequency stability without degrading the gain bandwidth of the amplifier. The complementary drive generator supplies current to the output transistors that swing from rail to rail.

Input

Input bias current (I_B) is minimized with cancellation circuitry on both input stages. The cancellation circuitry remains active when V_{CM} is more than 300mV from either rail. As V_{CM} approaches V^- the cancellation circuitry turns off and I_B is determined by the tail current of Q2 and the beta of the PNP input transistors. As V_{CM} approaches V^+ devices in the cancellation circuitry saturate causing I_B to increase (in the nanoamp range). Input offset voltage errors due to I_B can be minimized by equalizing the noninverting and inverting source impedances.
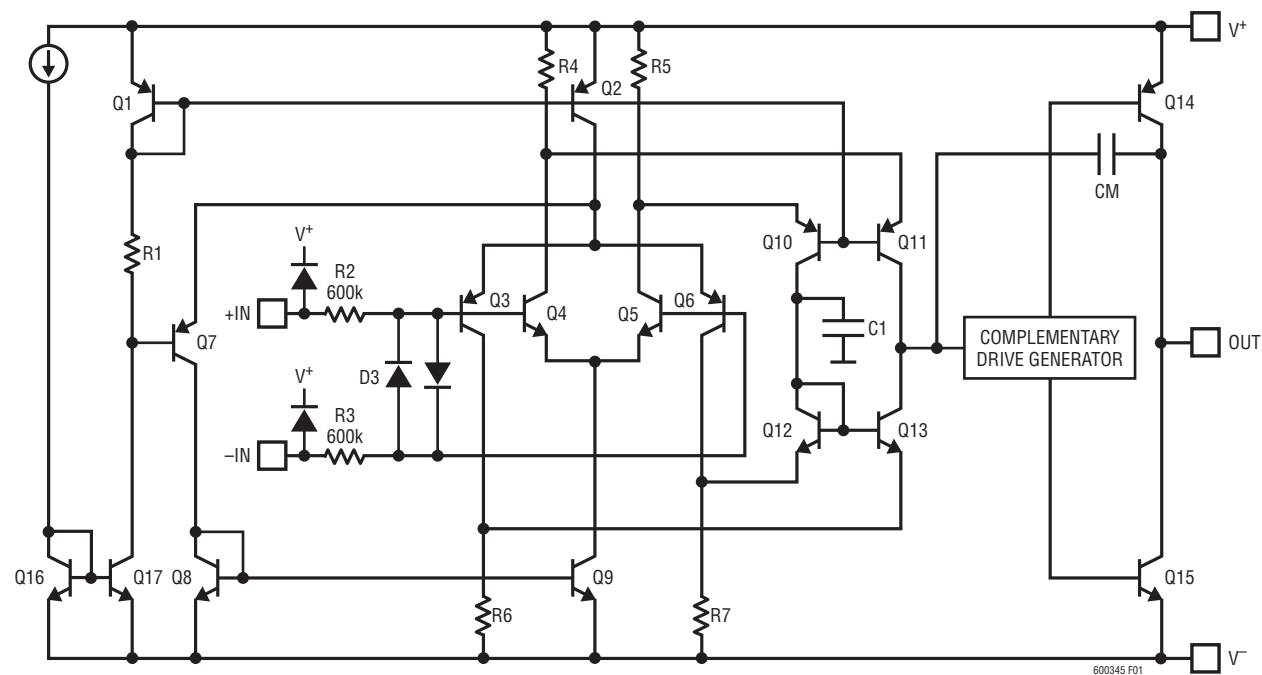
The input offset voltage changes depending on which input stage is active; input offset voltage is trimmed on both input stages, and is guaranteed to be 500µV max in the PNP stage. By trimming the input offset voltage of both input stages, the input offset voltage shift over the entire common mode range (CMRR) is typically 160µV, maintaining the precision characteristics of the amplifier.

The input stage of the LT6003/LT6004/LT6005 incorporates phase reversal protection to prevent wrong polarity outputs from occurring when the inputs are driven up to 9V below the negative rail. 600k protective resistors are included in the input leads so that current does not become excessive when the inputs are forced below V^- or when a large differential signal is applied. Input current should be limited to 10mA when the inputs are driven above the positive rail.

Output

The output of the LT6003/LT6004/LT6005 is guaranteed to swing within 100mV of the positive rail and 50mV of the negative rail with no load, over the industrial temperature range. The LT6003/LT6004/LT6005 can typically source 8mA on a single 5V supply. Sourcing current is reduced to 5mA on a single 1.8V supply as noted in the electrical characteristics. However, when sourcing more than 250µA with an output load impedance greater than 20kΩ, a 1µF capacitor in series with a 2k resistor should be placed from the output to ground to insure stability.

The normally reverse-biased substrate diode from the output to V^- will cause unlimited currents to flow when the output is forced below V^-. If the current is transient and limited to 100mA, no damage will occur.

APPLICATIONS INFORMATION

Gain

The open-loop gain is almost independent of load when the output is sourcing current. This optimizes performance in single supply applications where the load is returned to ground. The Typical Performance Characteristics curve of Open-Loop Gain for various loads shows the details.

Start-Up and Output Saturation Characteristics

Micropower op amps are often not micropower during start-up or during output saturation. This can wreak havoc on limited current supplies. In the worst case there may not be enough supply current available to take the system up to nominal voltages. Unlike the LT6003/LT6004/LT6005, when the output saturates, some op amps may draw excessive current and pull down the supplies, compromising rail-to-rail performance. Figure 2 shows the start-up characteristics of the LT6003/LT6004/LT6005 for three limiting cases. The circuits are shown in Figure 3. One circuit creates a positive offset forcing the output to come up saturated high. Another circuit creates a negative offset forcing the output to come up saturated low, while the last circuit brings the output up at 1/2 supply. In all cases, the supply current is well controlled and is not excessive when the output is on either rail.
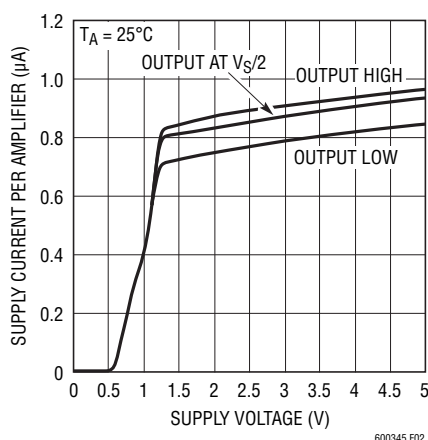
Figure 2. Start-Up Characteristics
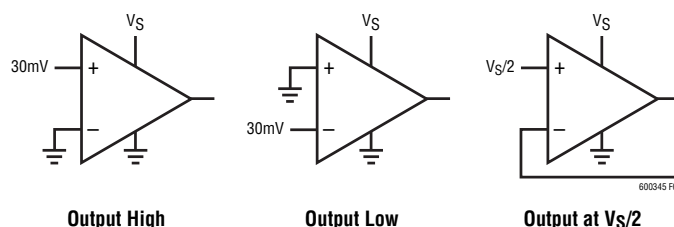
Figure 3. Circuits for Start-Up Characteristics

Adaptive Filter

The circuit of Figure 4 shows the LT6005 applied as a micropower adaptive filter, which automatically adjusts the time constant depending on the signal level. Op amp A1 buffers the input onto the RC which has either a 1ms or 20ms time constant depending on the state of switch S1. The signal is then buffered to the output by op amp A2. Op amps A3 and A4 are configured as gain-of-40 difference amplifiers, gaining up the difference between the buffered input voltage and the output. When there is no difference, the outputs of A3 and A4 will be near zero. When a positive signal step is applied to the input, the output of A3 rises. When a negative signal step is applied to the input, the output of A4 rises. These voltages are fed to the LT6700-2 comparator which has a built in 400mV reference. If the input step exceeds 10mV, the output of the difference amplifiers will exceed 400mV and the comparator output (wired in OR gate fashion) falls low. This turns on S1, reducing the time constant and speeding up the settling. The overall effect is that the circuit provides "slow filtering" with "fast settling." Waveforms for a 100mV input step are shown in the accompanying photo. The fast 1ms time constant is obvious in the output waveform, while the slow time constant is discernible as the slow ramping sections. That the slow time constant is discernible at all is due to delay time in the difference amplifier and comparator functions.

APPLICATIONS INFORMATION

ADAPTIVE FILTER IMPROVES INHERENT TRADE-OFF OF SETTLING TIME VS NOISE FILTERING. SMALL SIGNAL DC STEPS SETTLE WITH A 20ms TIME CONSTANT FOR AN 8Hz NOISE BANDWIDTH. LARGE STEP SIGNALS (>10mV) CAUSE S1 TO TURN ON, SPEEDING UP THE TIME CONSTANT TO 1ms, FOR IMPROVED SETTLING. AS THE OUTPUT SETTLES BACK TO WITHIN 10mV, 51 TURNS OFF AGAIN, RESTORING THE 20ms TIME CONSTANT, FOR IMPROVED FILTERING.

600345 F04

Figure 4. Adaptive Filter

$$I_{LOAD} = \frac{1.25V}{R1}$$

$$V_S = V_{LOAD} + 2V$$

Figure 5. Precision 1.25µA Current Source

PACKAGE DESCRIPTION

DC Package
4-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1724 Rev B)
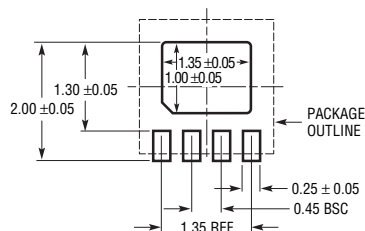
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDEDED

1.35 ±0.05
1.00 ±0.05
1.30 ±0.05
2.00 ±0.05
PACKAGE OUTLINE
0.25 ± 0.05
0.45 BSC
1.35 REF

2.00 ±0.10 (4 SIDES)
PIN 1 BAR TOP MARK (SEE NOTE 6)

0.200 REF
0.75 ±0.05
0.00 – 0.05

R = 0.05 TYP
R = 0.115 TYP
1.35 ± 0.10
1.00 ± 0.10
PIN 1 NOTCH R = 0.20 OR 0.25 × 45° CHAMFER
0.40 ±0.10
0.70 ±0.05
4
1
0.23 ± 0.05
0.45 BSC
1.35 REF

BOTTOM VIEW—EXPOSED PAD
(DC4) DFN 0309 REV B

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)

0.62 MAX
0.95 REF
1.22 REF
3.85 MAX 2.62 REF
1.4 MIN
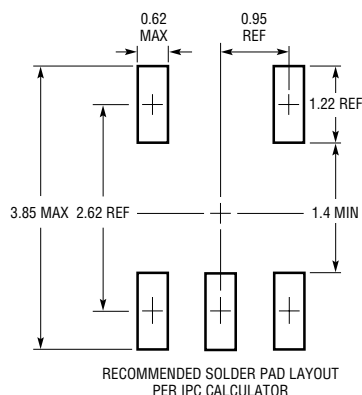
RECOMMENDED SOLDER PAD LAYOUT PER IPC CALCULATOR

2.90 BSC (NOTE 4)
2.80 BSC
1.50 – 1.75 (NOTE 4)
PIN ONE
0.95 BSC
0.30 – 0.45 TYP 5 PLCS (NOTE 3)

0.20 BSC
DATUM 'A'
0.30 – 0.50 REF
0.09 – 0.20 (NOTE 3)

0.80 – 0.90
1.00 MAX
0.01 – 0.10
1.90 BSC
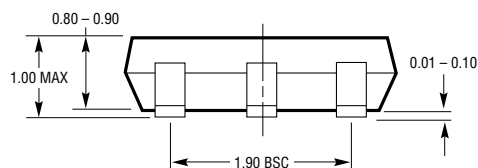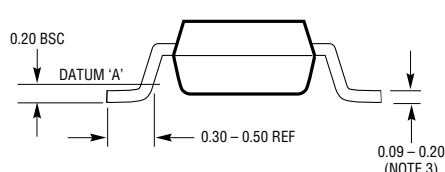
S5 TSOT-23 0302 REV B

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
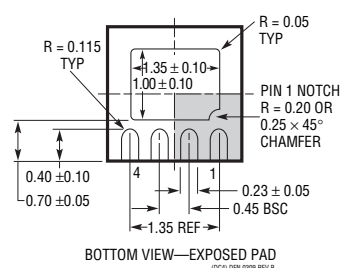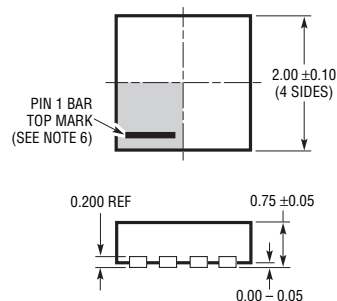6. JEDEC PACKAGE REFERENCE IS MO-193

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LINEAR TECHNOLOGY

PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

0.675 ±0.05

3.5 ±0.05

1.65 ±0.05
2.15 ±0.05
(2 SIDES)

PACKAGE OUTLINE

0.25 ± 0.05

0.50 BSC

2.38 ±0.05
(2 SIDES)

PIN 1 TOP MARK (NOTE 6)

3.00 ±0.10
(4 SIDES)

0.200 REF

0.75 ±0.05

0.00 – 0.05

R = 0.115 TYP

0.38 ± 0.10

1.65 ± 0.10
(2 SIDES)

0.25 ± 0.05

0.50 BSC

2.38 ±0.10
(2 SIDES)

BOTTOM VIEW—EXPOSED PAD

(DD) DFN 1203
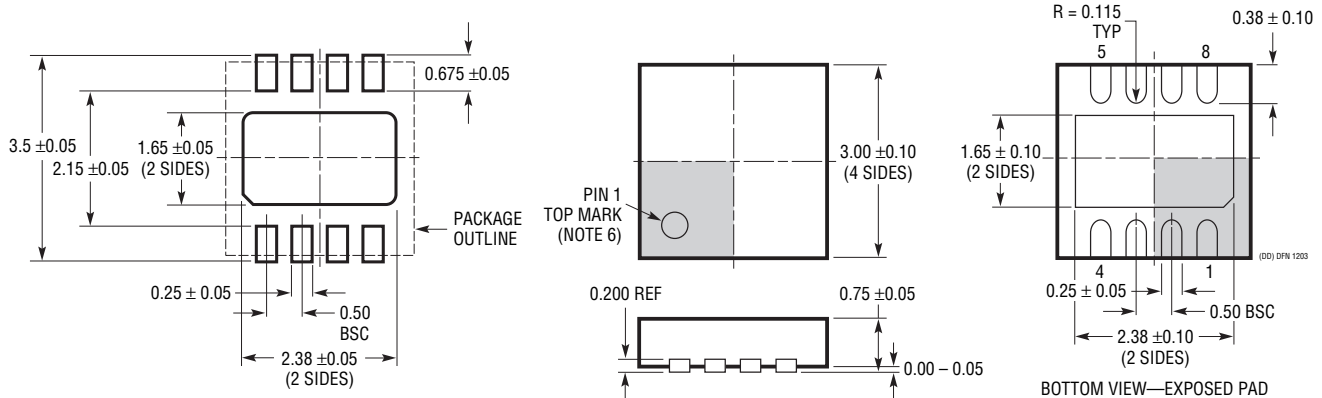
NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE MO-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON TOP AND BOTTOM OF PACKAGE

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)

RECOMMENDED SOLDER PAD LAYOUT

0.889 ± 0.127
(.035 ± .005)

5.23
(.206)
MIN

3.20 – 3.45
(.126 – .136)

0.42 ± 0.038
(.0165 ± .0015)
TYP

0.65
(.0256)
BSC

DETAIL "A"

0.254
(.010)

0° – 6° TYP

GAUGE PLANE

0.53 ± 0.152
(.021 ± .006)

DETAIL "A"

0.18
(.007)

3.00 ± 0.102
(.118 ± .004)
(NOTE 3)

8 7 6 5

0.52
(.0205)
REF

4.90 ± 0.152
(.193 ± .006)

3.00 ± 0.102
(.118 ± .004)
(NOTE 4)

1 2 3 4

1.10
(.043)
MAX

0.86
(.034)
REF

SEATING PLANE

0.22 – 0.38
(.009 – .015)
TYP

0.65
(.0256)
BSC

0.1016 ± 0.0508
(.004 ± .002)

MSOP (MS8) 0307 REV F
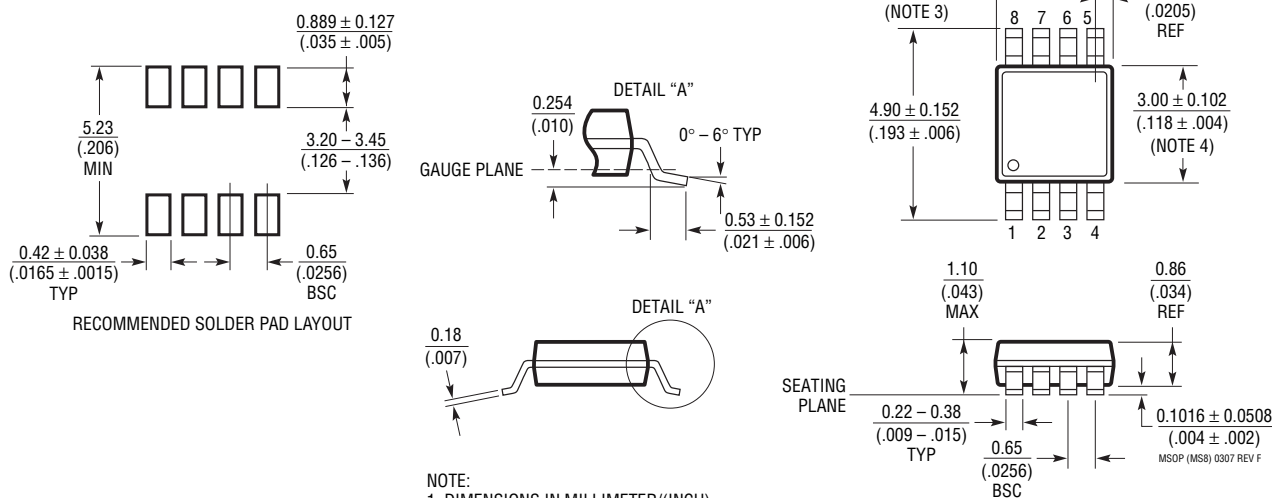
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

3.50 ±0.05
2.20 ±0.05
1.65 ±0.05 (2 SIDES)
0.65 ±0.05
0.25 ± 0.05
0.50 BSC
4.40 ±0.05 (2 SIDES)
PACKAGE OUTLINE

5.00 ±0.10 (2 SIDES)
3.00 ±0.10 (2 SIDES)
PIN 1 TOP MARK (SEE NOTE 6)
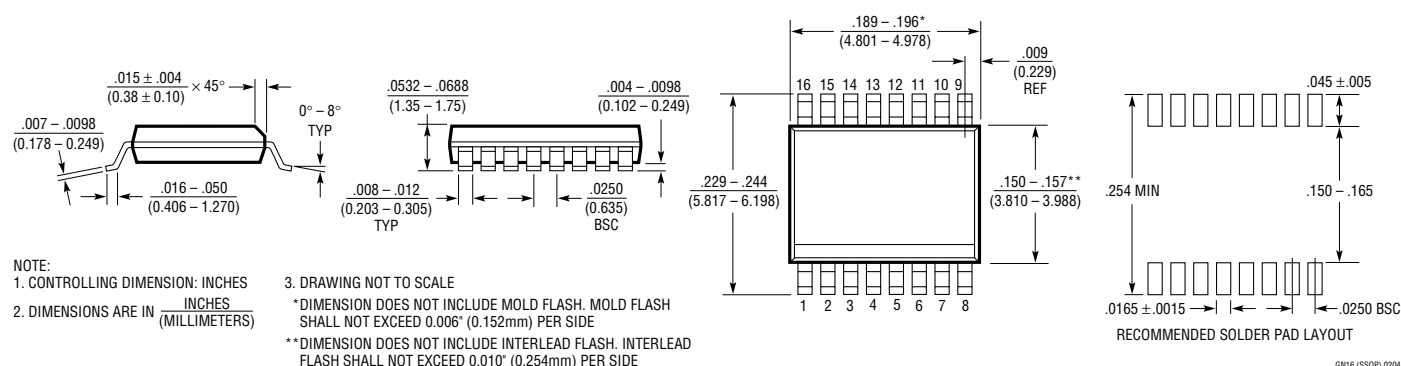0.200 REF
0.75 ±0.05
0.00 – 0.05

R = 0.115 TYP
0.40 ± 0.10
R = 0.20 TYP
1.65 ± 0.10 (2 SIDES)
9
16
8
1
PIN 1 NOTCH
0.25 ± 0.05
0.50 BSC
4.40 ±0.10 (2 SIDES)
BOTTOM VIEW—EXPOSED PAD
(DHC16) DFN 1103

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS

4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)

.015 ± .004 (0.38 ± 0.10) × 45°
0° – 8° TYP
.007 – .0098 (0.178 – 0.249)
.016 – .050 (0.406 – 1.270)
.0532 – .0688 (1.35 – 1.75)
.004 – .0098 (0.102 – 0.249)
.008 – .012 (0.203 – 0.305) TYP
.0250 (0.635) BSC

.189 – .196* (4.801 – 4.978)
.009 (0.229) REF
16 15 14 13 12 11 10 9
.229 – .244 (5.817 – 6.198)
.150 – .157** (3.810 – 3.988)
1 2 3 4 5 6 7 8

.045 ±.005
.254 MIN
.150 – .165
.0165 ±.0015
.0250 BSC
RECOMMENDED SOLDER PAD LAYOUT

GN16 (SSOP) 0204

NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$

3. DRAWING NOT TO SCALE
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

LINEAR TECHNOLOGY

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	3/11	Changed package description from TSSOP to SSOP in Description, Absolute Maximum Ratings, Pin Configuration, and Order Information	1 to 3

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Gain of –50 Ultralow Power Precision Gas Sensor Amplifier

CITY TECHNOLOGY
MODEL 40X(2)
OXYGEN SENSOR
BURNS 100µA IN AIR
(~21% O_2)

OXYGEN SENSOR

V_{OUT} = 500mV
IN AIR
(DURING READ PHASE)

GAIN = –50
V_{OS} = 5µV TYPICAL (INPUT REFERRED), AVERAGED
I_{SUPPLY} = 3µA
V_{SUPPLY} = ±0.9V TO ±2.7V

S1, S2: FAIRCHILD FSA1157 (NC)
S3: FAIRCHILD FSA1156 (NO)

CONNECT SWITCH GND PINS TO V_S^-

*20M FOR A_V = 1000
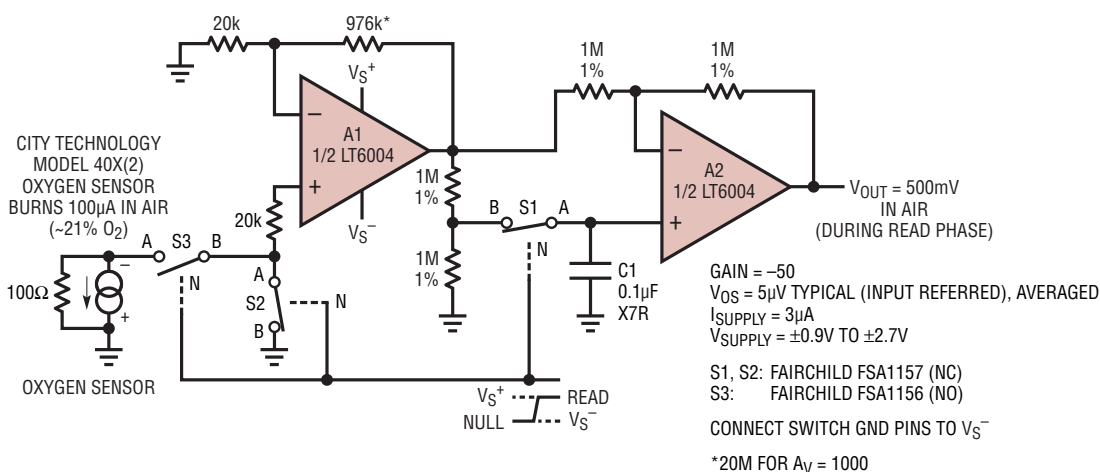
S1, S2 ARE NORMALLY CLOSED (N = LOW). S3 IS NORMALLY OPEN (N = LOW). A1's OUTPUT OFFSET IS STORED ON C1.
WHEN A READING IS DESIRED, SWITCHES REVERSE STATE, AND A2 ACTS AS A DIFFERENCE AMPLIFIER FROM THE STORED
OFFSET. NULL PHASE SHOULD BE ASSERTED 200ms OR MORE. A2 SETTLES 50ms AFTER READ PHASE IS ASSERTED, WITH
WORST CASE ROOM TEMPERATURE DROOP RATE IS 0.8µV/ms DOMINATED BY ANALOG SWITCH LEAKAGE CURRENT.

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RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1490A/LT1491A	50µA Dual/Quad Over-The-Top® Rail-to-Rail Input and Output Op Amps	950µV $V_{OS(MAX)}$, Gain Bandwidth = 200kHz
LT1494/LT1495/LT1496	1.5µA Max Single/Dual/Quad Over-The-Top Precision Rail-to-Rail Input and Output Op Amps	375µV $V_{OS(MAX)}$, Gain Bandwidth = 2.7kHz
LT1672/LT1673/LT1674	2µA Max, AV ≥ 5, Single/Dual/Quad Over-The-Top Precision Rail-to-Rail Input and Output Op Amps	Gain of 5 Stable, Gain Bandwidth = 12kHz
LT1782	Micropower, Over-The-Top, SOT-23, Rail-to-Rail Input and Output Op Amps	SOT-23, 800µV $V_{OS(MAX)}$, I_S = 55µA$_{(MAX)}$, Gain Bandwidth = 200kHz, Shutdown Pin
LT2178/LT2179	17µA Dual/Quad Single Supply Op Amps	120µV $V_{OS(MAX)}$, Gain Bandwidth = 60kHz
LT6000/LT6001/LT6002	1.8V, 16µA Max Single/Dual/Quad Precision Rail-to-Rail Op Amps	600µV $V_{OS(MAX)}$, Gain Bandwidth = 50kHz, Shutdown

Over-The-Top is a registered trademark of Linear Technology Corporation.

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