# LINEAR TECHNOLOGY

# 60V Synchronous 4-Switch Buck-Boost Controller

## FEATURES

- **4-Switch Single Inductor Architecture Allows $V_{IN}$ Above, Below or Equal to $V_{OUT}$**
- **Synchronous Switching: Up to 98.5% Efficiency**
- **Wide $V_{IN}$ Range: 4.7V to 60V**
- **2% Output Voltage Accuracy: $1.2V \leq V_{OUT} < 60V$**
- **6% Output Current Accuracy: $0V \leq V_{OUT} < 60V$**
- Input and Output Current Regulation with Current Monitor Outputs
- No Top FET Refresh in Buck or Boost
- $V_{OUT}$ Disconnected from $V_{IN}$ During Shutdown
- C/10 Charge Termination and Output Shorted Flags
- Capable of 100W or Greater per IC
- Easy Parallel Capability to Extend Output Power
- 38-Lead TSSOP with Exposed Pad

## APPLICATIONS

- Automotive, Telecom, Industrial Systems
- High Power Battery-Powered System

## DESCRIPTION

The LT®3790 is a synchronous 4-switch buck-boost voltage/current regulator controller. The LT3790 can regulate output voltage, output current, or input current with input voltages above, below, or equal to the output voltage. The constant-frequency, current mode architecture allows its frequency to be adjusted or synchronized from 200kHz to 700kHz. No top FET refresh switching cycle is needed in buck or boost operation. With 60V input, 60V output capability and seamless transitions between operating regions, the LT3790 is ideal for voltage regulator, battery/super-capacitor charger applications in automotive, industrial, telecom, and even battery-powered systems.

The LT3790 provides input current monitor, output current monitor, and various status flags, such as C/10 charge termination and shorted output flag.
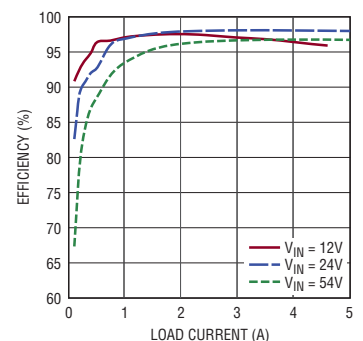
## TYPICAL APPLICATION

### 120W (24V 5A) Buck-Boost Voltage Regulator
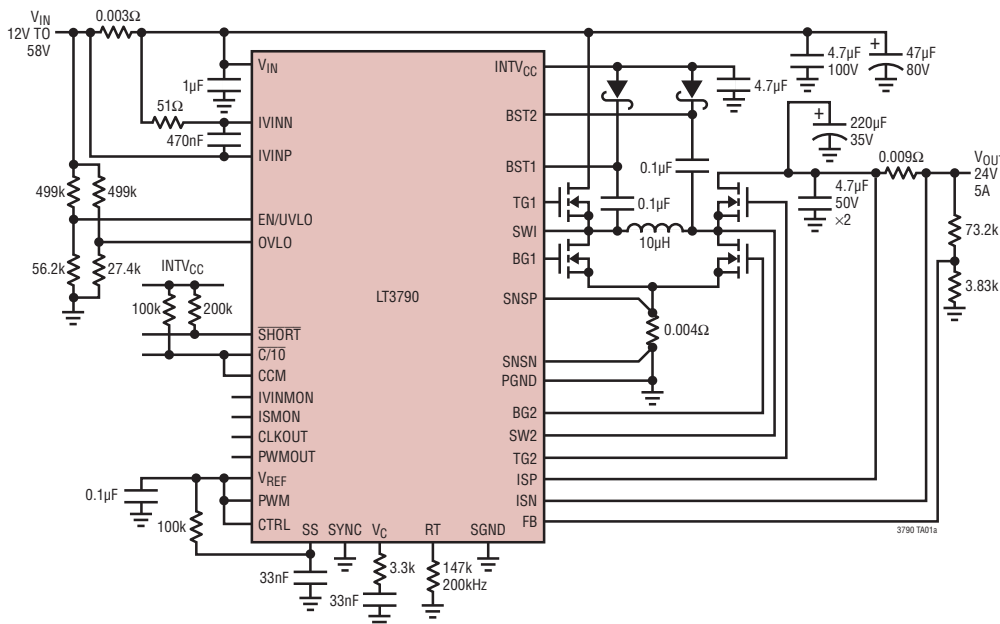


Efficiency vs Load Current

# ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Supply Voltages

Input Supply ($V_{IN}$).....................................................60V

SW1, SW2................................................. −5V to 60V

$\overline{C/10}$, $\overline{SHORT}$ ............................................................15V

EN/UVLO, IVINP, IVINN, ISP, ISN ..............................60V

$INTV_{CC}$, (BST1-SW1), (BST2-SW2)............................6V

CCM, SYNC, RT, CTRL, OVLO, PWM .........................6V

IVINMON, ISMON, FB, SS, VC, $V_{REF}$ .........................6V

IVINP-IVINN, ISP-ISN, SNSP-SNSN......................±0.5V

SNSP, SNSN.........................................................±0.3V

Operating Junction Temperature (Notes 2, 3)

    LT3790E/LT3790I .............................. −40°C to 125°C

    LT3790H.......................................... −40°C to 150°C

    LT3790MP ....................................... −55°C to 150°C

Storage Temperature Range .................. −65°C to 150°C

Lead Temperature (Soldering, 10 sec)...................300°C

# PIN CONFIGURATION

TOP VIEW

| | | |
|---|---|---|
| CTRL | 1 | 38 OVLO |
| SS | 2 | 37 FB |
| PWM | 3 | 36 $V_C$ |
| $\overline{C/10}$ | 4 | 35 RT |
| $\overline{SHORT}$ | 5 | 34 SYNC |
| $V_{REF}$ | 6 | 33 CLKOUT |
| ISMON | 7 | 32 CCM |
| IVINMON | 8 | 31 PWMOUT |
| EN/UVLO | 9 | 30 SGND |
| IVINP | 10 | 29 TEST1 |
| IVINN | 11 | 28 SNSN |
| $V_{IN}$ | 12 | 27 SNSP |
| $INTV_{CC}$ | 13 | 26 ISN |
| TG1 | 14 | 25 ISP |
| BST1 | 15 | 24 TG2 |
| SW1 | 16 | 23 NC |
| PGND | 17 | 22 BST2 |
| BG1 | 18 | 21 SW2 |
| BG2 | 19 | 20 PGND |

39 SGND

FE PACKAGE
38-LEAD PLASTIC TSSOP

$\theta_{JA}$ = 28°C/W
EXPOSED PAD (PIN 39) IS SGND, MUST BE SOLDERED TO PCB
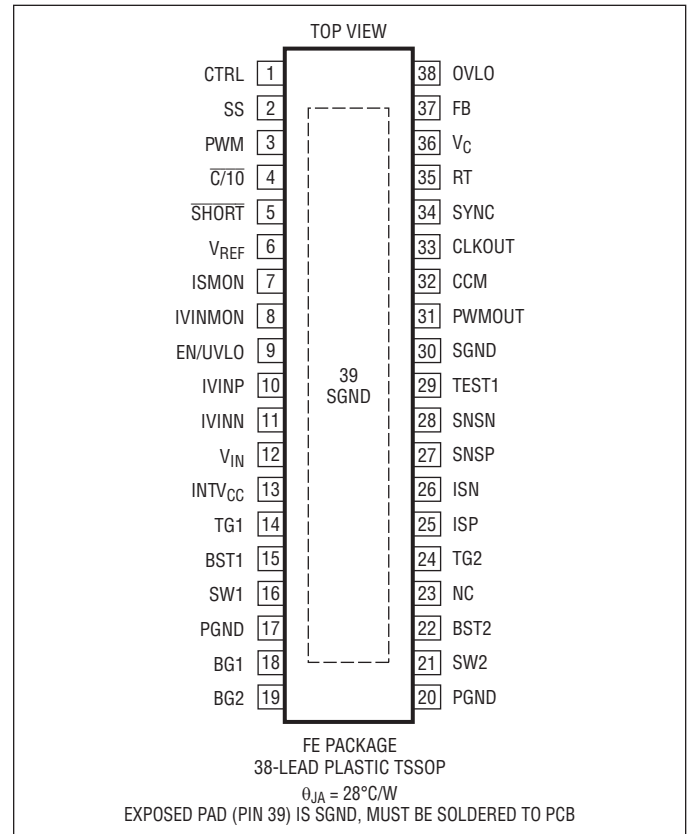
# ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LT3790EFE#PBF | LT3790EFE#TRPBF | LT3790FE | 38-Lead Plastic TSSOP | −40°C to 125°C |
| LT3790IFE#PBF | LT3790IFE#TRPBF | LT3790FE | 38-Lead Plastic TSSOP | −40°C to 125°C |
| LT3790HFE#PBF | LT3790HFE#TRPBF | LT3790FE | 38-Lead Plastic TSSOP | −40°C to 150°C |
| LT3790MPFE#PBF | LT3790MPFE#TRPBF | LT3790FE | 38-Lead Plastic TSSOP | −55°C to 150°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

# ELECTRICAL CHARACTERISTICS   The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 2). $V_{IN}$ = 12V, $V_{EN/UVLO}$ = 12V unless otherwise noted.

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| $V_{IN}$ Operating Voltage | | | 4.7 | | 60 | V |
| $V_{IN}$ Shutdown $I_Q$ | $V_{EN/UVLO}$ = 0V | | | 0.1 | 1 | µA |
| $V_{IN}$ Operating $I_Q$ (Not Switching) | FB = 1.3V, $R_T$ = 59.0k | | | 3.0 | 4 | mA |

3790fa

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 2). $V_{IN}$ = 12V, $V_{EN/UVLO}$ = 12V unless otherwise noted.

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Logic Inputs** | | | | | | |
| EN/UVLO Falling Threshold | | ● | 1.16 | 1.2 | 1.24 | V |
| EN/UVLO Rising Hysteresis | | | | 15 | | mV |
| EN/UVLO Input Low Voltage | $I_{VIN}$ Drops Below 1µA | | | | 0.3 | V |
| EN/UVLO Pin Bias Current Low | $V_{EN/UVLO}$ = 1V | | 2 | 3 | 4 | µA |
| EN/UVLO Pin Bias Current High | $V_{EN/UVLO}$ = 1.6V | | | 10 | 100 | nA |
| CCM Threshold Voltage | | | 0.3 | | 1.5 | V |
| CTRL Input Bias Current | $V_{CTRL}$ = 1V | | | 20 | 50 | nA |
| CTRL Latch-Off Threshold | Rising | | 45 | 50 | 55 | mV |
| CTRL Latch-Off Hysteresis | | | | 13 | | mV |
| OVLO Rising Shutdown Voltage | | ● | 2.85 | 3 | 3.15 | V |
| OVLO Falling Hysteresis | | | | 75 | | mV |
| **Regulation** | | | | | | |
| $V_{REF}$ Voltage | | ● | 1.96 | 2.00 | 2.04 | V |
| $V_{REF}$ Line Regulation | 4.7V < $V_{IN}$ < 60V | | | 0.002 | 0.04 | %/V |
| $V_{(ISP-ISN)}$ Threshold | $V_{CTRL}$ = 2V, $V_{ISP}$ = 12V/0.1V | | 58 | 60 | 62 | mV |
| | | ● | 56 | 60 | 64 | mV |
| | $V_{CTRL}$ = 1V, $V_{ISP}$ = 12V/0.1V | | 48 | 50 | 52 | mV |
| | | ● | 46 | 50 | 54 | mV |
| | $V_{CTRL}$ = 600mV, $V_{ISP}$ = 12V/0.1V | | 28 | 30 | 32 | mV |
| | | ● | 26 | 30 | 34 | mV |
| | $V_{CTRL}$ = 100mV, $V_{ISP}$ = 12V/0.1V | | 1 | 4.2 | 7.4 | mV |
| | | ● | 0.2 | 4.2 | 8.2 | mV |
| ISP Bias Current | $V_{ISP}$ = 12V, $V_{ISN}$ = 11.9V | | | 110 | | µA |
| ISN Bias Current | $V_{ISP}$ = 12V, $V_{ISN}$ = 11.9V | | | 20 | | µA |
| Output Current Sense Common Mode Range | | | 0 | | 60 | V |
| Output Current Sense Amplifier $g_m$ | | | | 1650 | | µS |
| ISMON Monitor Voltage | $V_{(ISP-ISN)}$ = 60mV | ● | 1.14 | 1.2 | 1.26 | V |
| Input Current Sense Threshold $V_{(IVINP-IVINN)}$ | 3V ≤ $V_{IVINP}$ ≤ 60V | ● | 46.5 | 50 | 54 | mV |
| IVINP Bias Current | $V_{IVINP}$ = $V_{IVINN}$ = 12V | | | 90 | | µA |
| IVINN Bias Current | $V_{IVINP}$ = $V_{IVINN}$ = 12V | | | 20 | | µA |
| Input Current Sense Common Mode Range | | | 3 | | 60 | V |
| Input Current Sense Amplifier $g_m$ | | | | 2.12 | | mS |
| IVINMON Monitor Voltage | $V_{(IVINP-IVINN)}$ = 50mV | ● | 0.96 | 1 | 1.04 | V |
| FB Regulation Voltage | | | 1.194 | 1.2 | 1.206 | V |
| | | ● | 1.176 | 1.2 | 1.220 | V |
| FB Line Regulation | 4.7V < $V_{IN}$ < 60V | | | 0.002 | 0.025 | %/V |
| FB Amplifier $g_m$ | | | | 565 | | µS |
| FB Pin Input Bias Current | FB in Regulation | | | 100 | 200 | nA |
| $V_C$ Standby Input Bias Current | PWM = 0V | | −20 | | 20 | nA |
| $V_{SENSE(MAX)}$ ($V_{SNSP-SNSN}$) | Boost | ● | 42 | 51 | 60 | mV |
| | Buck | ● | −56 | −47.5 | −39 | mV |
| **Fault** | | | | | | |
| SS Pull-Up Current | $V_{SS}$ = 0V | | | 14 | | µA |
| SS Discharge Current | | | | 1.4 | | µA |

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# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 2). $V_{IN}$ = 12V, $V_{EN/UVLO}$ = 12V unless otherwise noted.

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $\overline{C/10}$ Falling Threshold ($V_{(ISP-ISN)}$) | $V_{FB}$ = 1.2V | | 1 | 5 | 9 | mV |
| $\overline{SHORT}$ Falling Threshold ($V_{FB}$) | | | 380 | 400 | 450 | mV |
| $\overline{C/10}$ Pin Output Impedance | | | | 1.1 | 2.0 | kΩ |
| $\overline{SHORT}$ Pin Output Impedance | | | | 1.1 | 2.0 | kΩ |
| SS Latch-Off Threshold | | | | 1.75 | | V |
| SS Reset Threshold | | | | 0.2 | | V |
| **Oscillator** | | | | | | |
| Switching Frequency | $R_T$ = 147k<br>$R_T$ = 59.0k<br>$R_T$ = 29.1k | | 190<br>380<br>665 | 200<br>400<br>700 | 210<br>420<br>735 | kHz<br>kHz<br>kHz |
| SYNC Frequency | | | 200 | | 700 | kHz |
| SYNC Pin Resistance to GND | | | | 90 | | kΩ |
| SYNC Threshold Voltage | | | 0.3 | | 1.5 | V |
| **Internal $V_{CC}$ Regulator** | | | | | | |
| INTV$_{CC}$ Regulation Voltage | | | 4.8 | 5 | 5.2 | V |
| Dropout ($V_{IN}$ – INTV$_{CC}$) | $I_{INTVCC}$ = –10mA, $V_{IN}$ = 5V | | | 240 | 350 | mV |
| INTV$_{CC}$ Undervoltage Lockout | | | 3.1 | 3.5 | 3.9 | V |
| INTV$_{CC}$ Current Limit | $V_{INTVCC}$ = 4V | | | 67 | | mA |
| **PWM** | | | | | | |
| PWM Threshold Voltage | | | 0.3 | | 1.5 | V |
| PWM Pin Resistance to GND | | | | 90 | | kΩ |
| PWMOUT Pull-Up Resistance | | | | 10 | 20 | Ω |
| PWMOUT Pull-Down Resistance | | | | 5 | 10 | Ω |
| **NMOS Drivers** | | | | | | |
| TG1, TG2 Gate Driver On-Resistance<br>    Gate Pull-Up<br>    Gate Pull-Down | $V_{BST}$ – $V_{SW}$ = 5V | | | <br>2.6<br>1.7 | | <br>Ω<br>Ω |
| BG1, BG2 Gate Driver On-Resistance<br>    Gate Pull-Up<br>    Gate Pull-Down | $V_{INTVCC}$ = 5V | | | <br>3<br>1.2 | | <br>Ω<br>Ω |
| TG Off to BG On Delay | $C_L$ = 3300pF | | | 60 | | ns |
| BG Off to TG On Delay | $C_L$ = 3300pF | | | 60 | | ns |
| TG1, TG2, $t_{OFF(MIN)}$ | $R_T$ = 59.0k | | | 240 | 320 | ns |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LT3790E is guaranteed to meet performance from 0°C to 125°C junction temperature. Specification over the -40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3790I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range. The LT3790H is guaranteed to meet performance specifications over the –40°C to 150°C

operating junction temperature range. The LT3790MP is guaranteed to meet performance specifications over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

**Note 3:** The LT3790 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability.

# TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

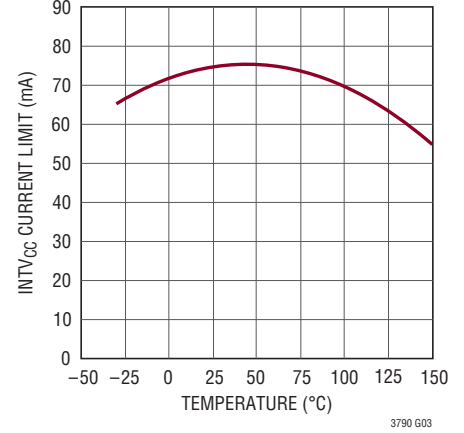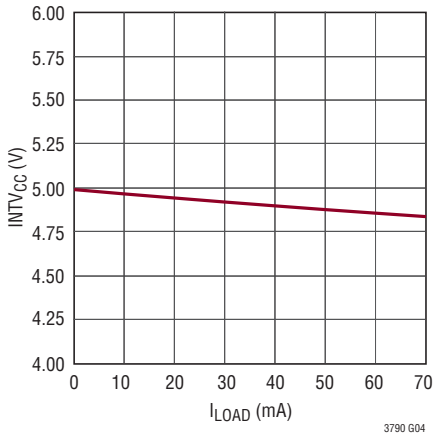**INTV$_{CC}$ Dropout Voltage vs Current, Temperature**
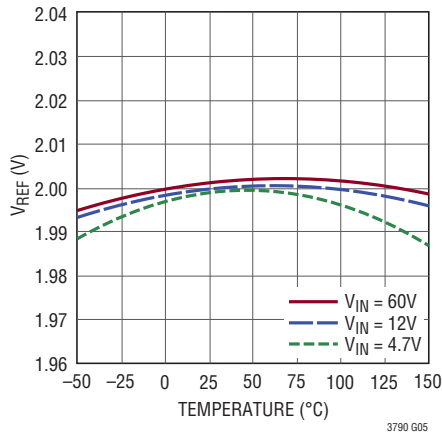


3790 G01
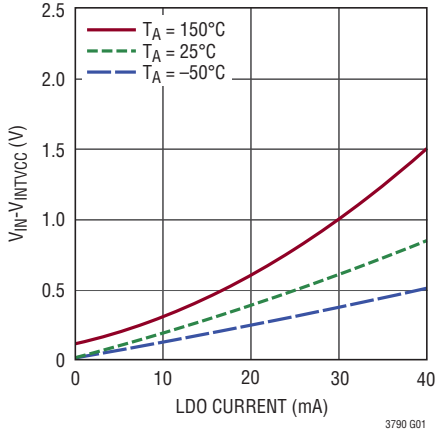
**INTV$_{CC}$ Voltage vs Temperature**



3790 G02
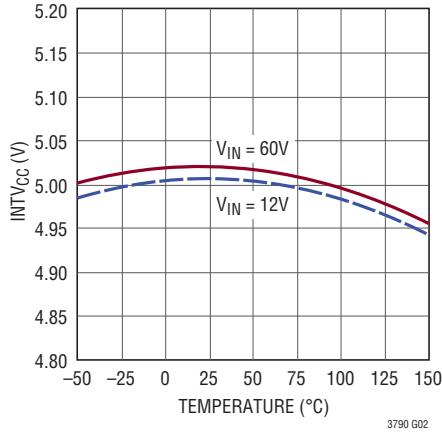
**INTV$_{CC}$ Current Limit vs Temperature**



3790 G03

**INTV$_{CC}$ Load Regulation**



3790 G04
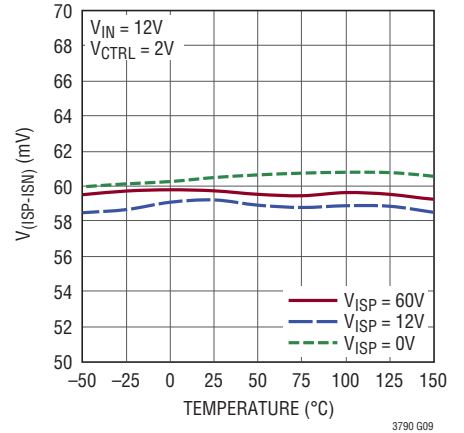
**V$_{REF}$ Voltage vs Temperature**



3790 G05

**V$_{REF}$ Load Regulation**



3790 G06

**V$_{(ISP-ISN)}$ Threshold vs V$_{CTRL}$**



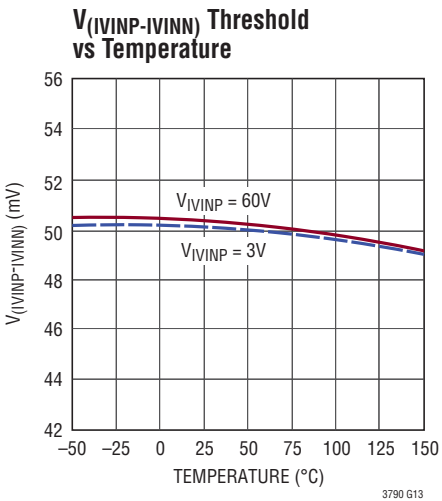3790 G07
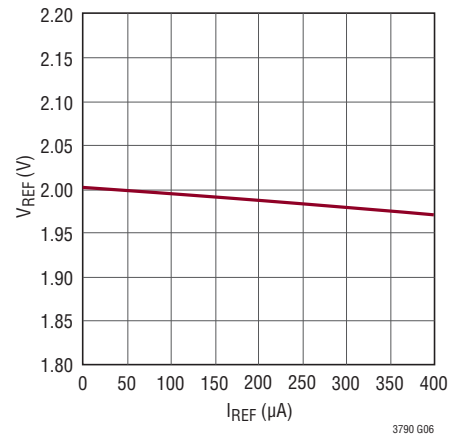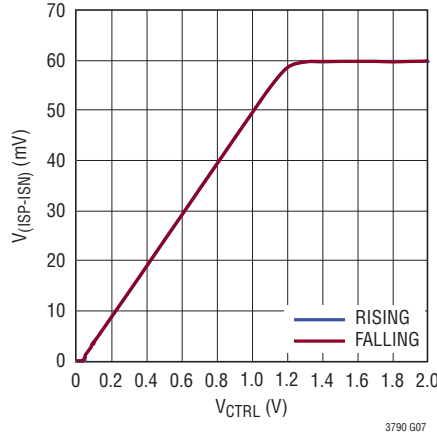
**V$_{(ISP-ISN)}$ Threshold vs V$_{ISP}$**



3790 G08

**V$_{(ISP-ISN)}$ Threshold vs Temperature**



3790 G09

For more information www.linear.com/LT3790
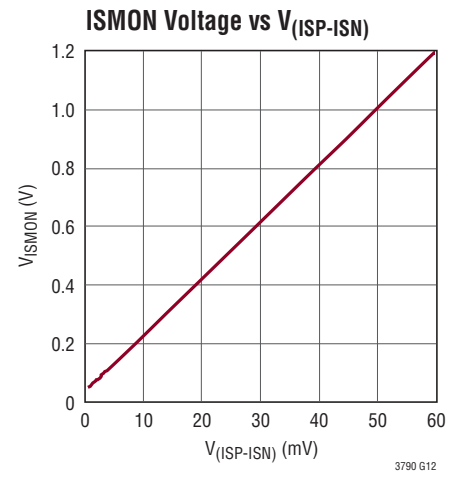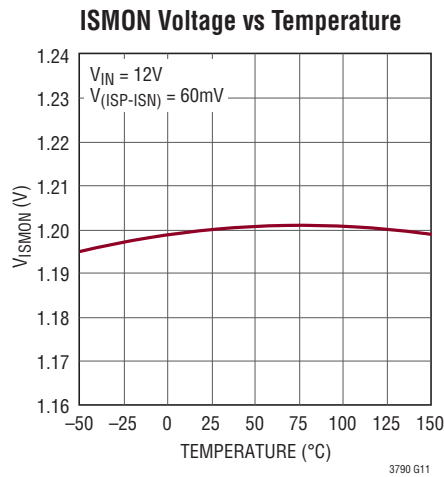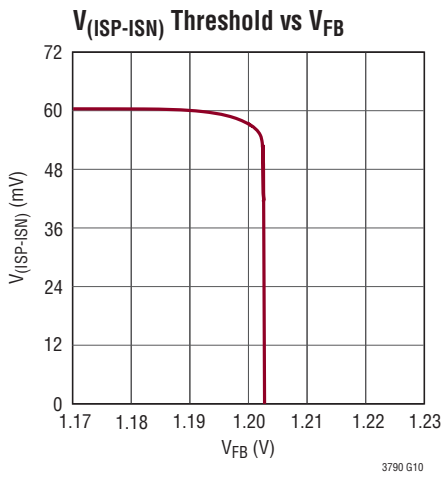
# TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

**$V_{(ISP-ISN)}$ Threshold vs $V_{FB}$**

3790 G10

**ISMON Voltage vs Temperature**

$V_{IN}$ = 12V
$V_{(ISP-ISN)}$ = 60mV

3790 G11

**ISMON Voltage vs $V_{(ISP-ISN)}$**

3790 G12

**$V_{(IVINP-IVINN)}$ Threshold vs Temperature**

$V_{IVINP}$ = 60V
$V_{IVINP}$ = 3V

3790 G13

**$V_{(IVINP-IVINN)}$ Threshold vs $V_{IVINP}$**

3790 G14

**IVINMON Voltage vs Temperature**

$V_{IVINP}$ = 12V
$V_{(IVINP-IVINN)}$ = 50mV

3790 G15

**$V_{(IVINP-IVINN)}$ Threshold vs $V_{FB}$**

3790 G16

**FB Regulation Voltage vs Temperature**

$V_{IN}$ = 60V
$V_{IN}$ = 12V
$V_{IN}$ = 4.7V

3790 G17

**$\overline{SHORT}$ Threshold vs Temperature**

RISING
FALLING

3790 G18

3790fa

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# TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

**OVLO Threshold vs Temperature**



**Soft-Start Current vs Temperature**



**Supply Current vs Input Voltage**



**EN/UVLO Pin Current**



**EN/UVLO Threshold Voltage**



**Oscillator Frequency vs Temperature**



**TG1, TG2 Minimum On-Time vs Temperature**



**TG1, TG2 Minimum Off-Time vs Temperature**



**$V_{(BST1-SW1)}$, $V_{(BST2-SW2)}$ UVLO vs Temperature**
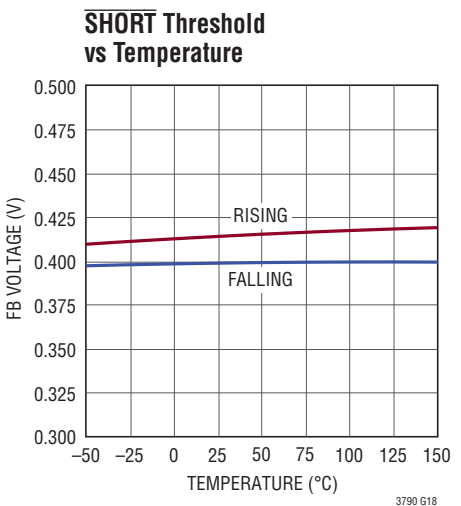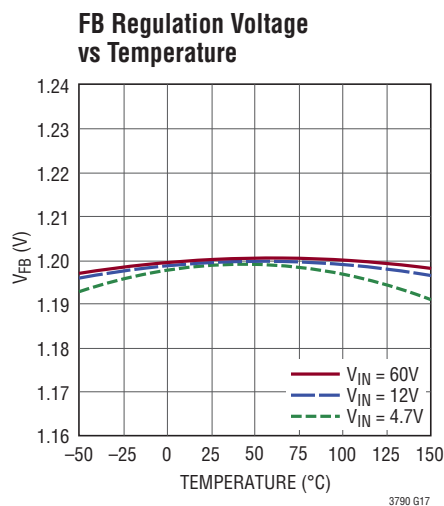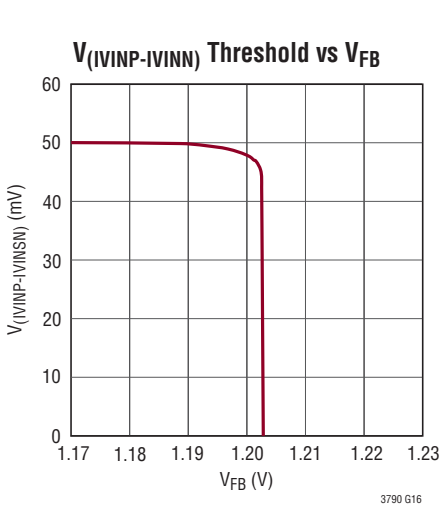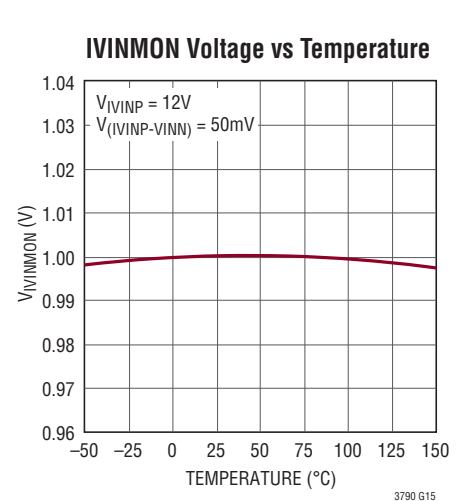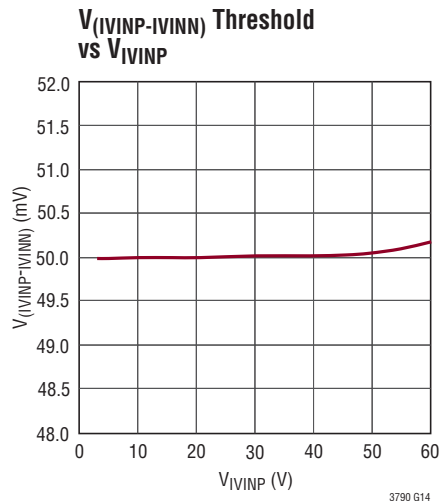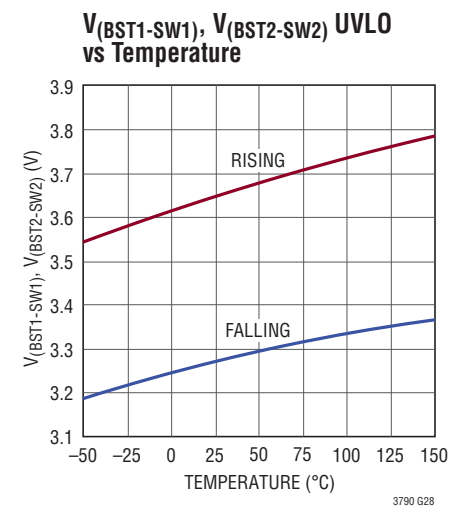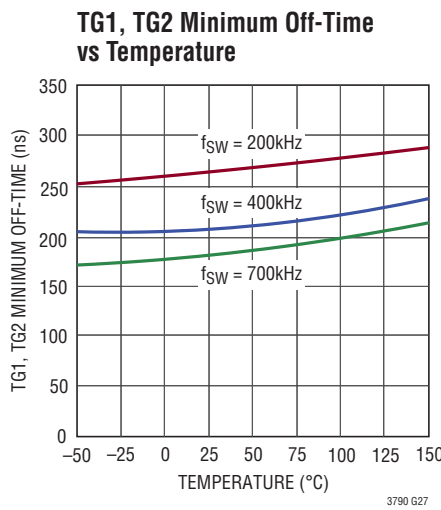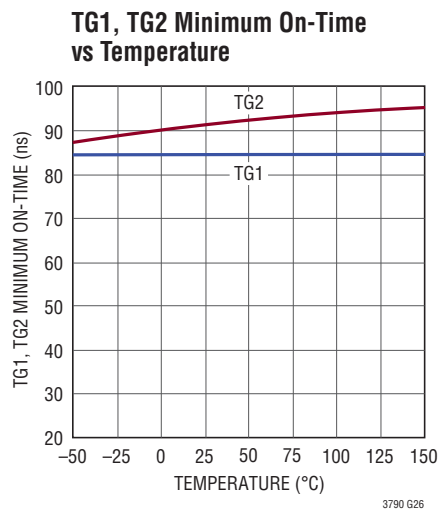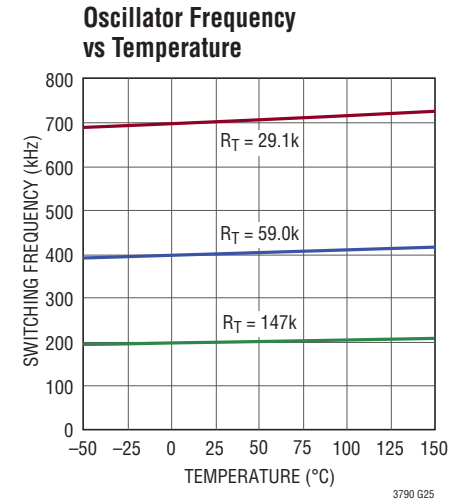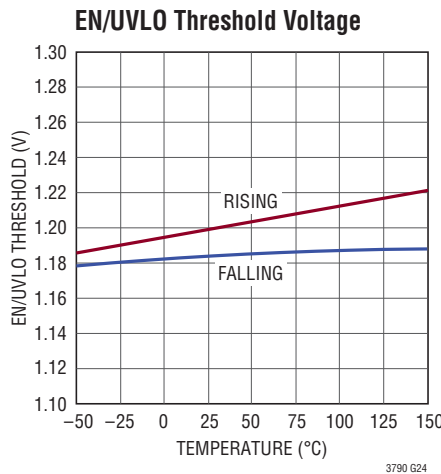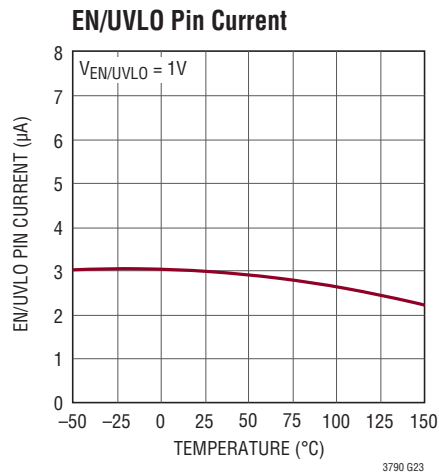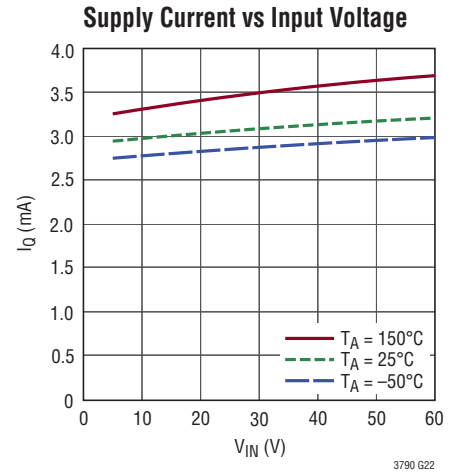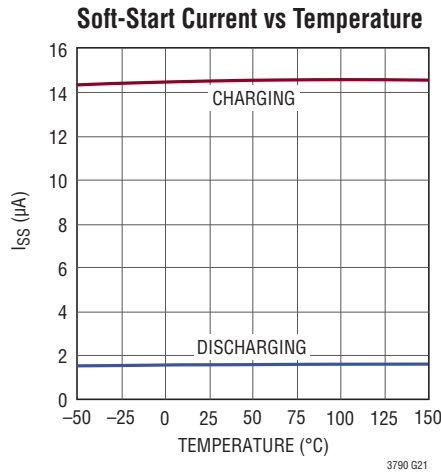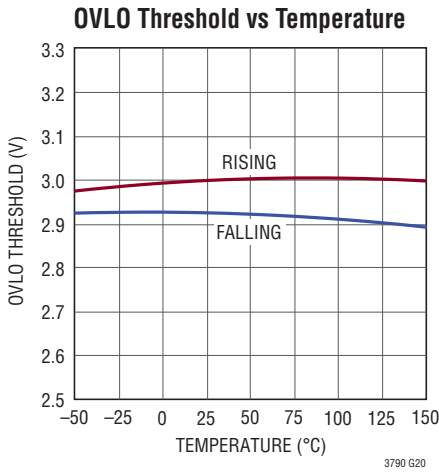
# TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

**BG1, BG2 Driver On-Resistance vs Temperature**
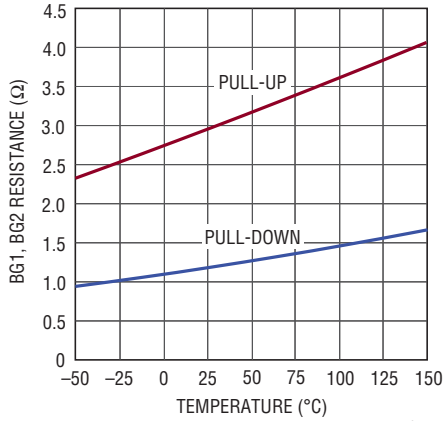


3790 G29

**TG1, TG2 Driver On-Resistance vs Temperature**
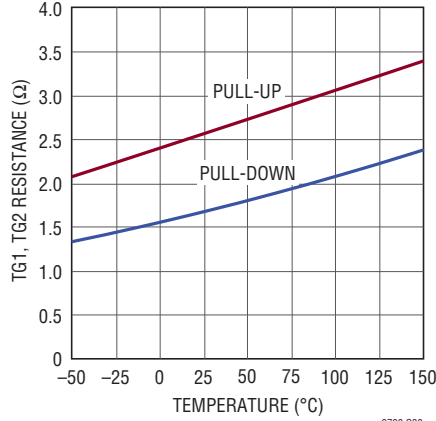


3790 G30

**PWMOUT On-Resistance vs Temperature**
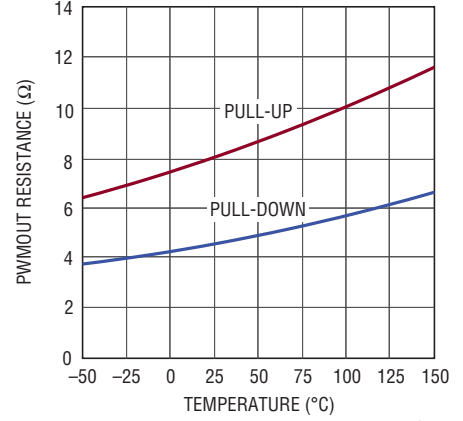


3790 G31

**$V_C$ Voltage vs Duty Cycle**
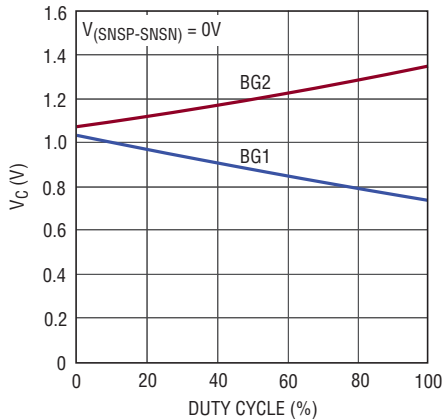


3790 G32

**$V_{(SNSP-SNSN)}$ Buck Threshold vs $V_C$**
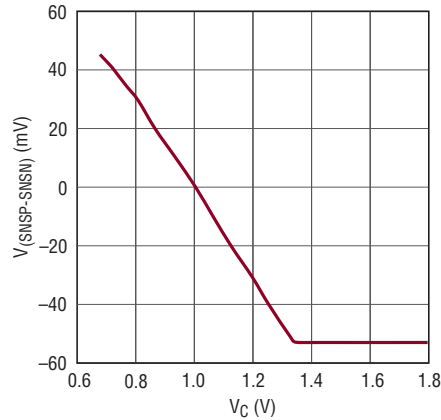


3790 G33

**$V_{(SNSP-SNSN)}$ Buck Threshold vs Temperature**
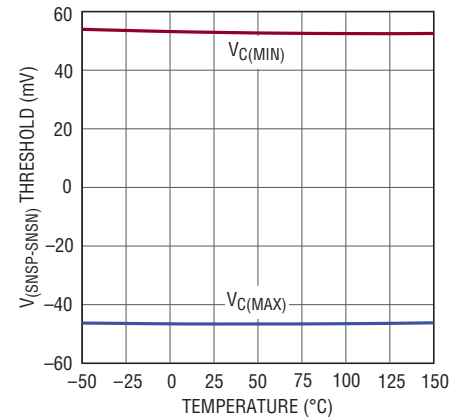


3790 G34

**$V_{(SNSP-SNSN)}$ Boost Threshold vs $V_C$**
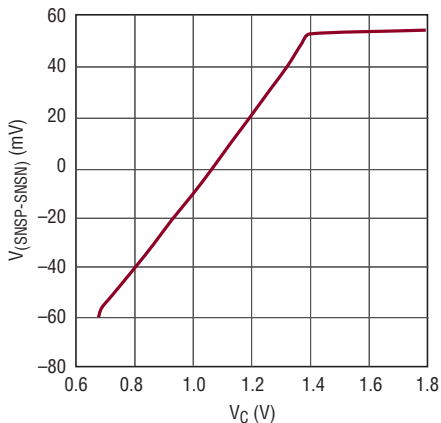


3790 G35

**$V_{(SNSP-SNSN)}$ Boost Threshold vs Temperature**



3790 G36

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8
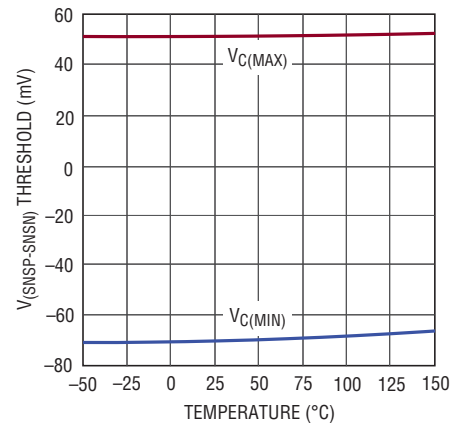
# PIN FUNCTIONS

**CTRL (Pin 1):** Output Current Sense Threshold Adjustment Pin. Regulating threshold $V_{(ISP-ISN)}$ is 1/20th of $V_{CTRL}$. CTRL linear range is from 0V to 1.1V. For $V_{CTRL} > 1.3V$, the current sense threshold is constant at the full-scale value of 60mV. For $1.1V < V_{CTRL} < 1.3V$, the dependence of the current sense threshold upon $V_{CTRL}$ transitions from a linear function to a constant value, reaching 98% of full scale by $V_{CTRL} = 1.2V$. Connect CTRL to $V_{REF}$ for the 60mV default threshold. Force less than 50mV (typical) to stop switching. Do not leave this pin open.

**SS (Pin 2):** Soft-start reduces the input power sources surge current by gradually increasing the controller's current limit. A minimum value of 22nF is recommended on this pin. A 100k resistor must be placed between SS and $V_{REF}$ for the LT3790.

**PWM (Pin 3):** A signal low turns off switches, idles switching and disconnects the $V_C$ pin from all external loads. The PWMOUT pin follows the PWM pin. PWM has an internal 90k pull-down resistor. If not used, connect to $INTV_{CC}$.

**$\overline{C/10}$ (Pin 4):** C/10 Charge Termination Pin. An open-drain pull-down on $\overline{C/10}$ asserts if $V_{(ISP-ISN)}$ is less than 5mV (typical). To function, the pin requires an external pull-up resistor.

**$\overline{SHORT}$ (Pin 5):** Output Shorted Pin. An open-drain pull-down on $\overline{SHORT}$ asserts if FB is less than 400mV (typical) and $V_{(ISP-ISN)}$ is larger than 5mV (typical). To function, the pin requires an external pull-up resistor.

**$V_{REF}$ (Pin 6):** Voltage Reference Output Pin, Typically 2V. This pin drives a resistor divider for the CTRL pin, either for output current adjustment or for temperature limit/compensation of the output load. Can supply up to 200µA of current.

**ISMON (Pin 7):** Monitor pin that produces a voltage that is twenty times the voltage $V_{(ISP-ISN)}$. ISMON will equal 1.2V when $V_{(ISP-ISN)} = 60mV$. For parallel applications, tie master LT3790 ISMON pin to slave LT3790 CTRL pin.

**IVINMON (Pin 8):** Monitor pin that produces a voltage that is twenty times the voltage $V_{(IVINP-IVINN)}$. IVINMON will equal 1V when $V_{(IVINP-IVINN)} = 50mV$.

**EN/UVLO (Pin 9):** Enable Control Pin. Forcing an accurate 1.2V falling threshold with an externally programmable hysteresis is generated by the external resistor divider and a 3µA pull-down current. Above the 1.2V (typical) threshold (but below 6V), EN/UVLO input bias current is sub-µA. Below the falling threshold, a 3µA pull-down current is enabled so the user can define the hysteresis with the external resistor selection. An undervoltage condition resets soft-start. Tie to 0.3V, or less, to disable the device and reduce $V_{IN}$ quiescent current below 1µA.

**IVINP (Pin 10):** Positive Input for the Input Current Limit and Monitor. Input bias current for this pin is typically 90µA.

**IVINN (Pin 11):** Negative Input for the Input Current Limit and Monitor. The input bias current for this pin is typically 20µA.

**$V_{IN}$ (Pin 12):** Main Input Supply. Bypass this pin to PGND with a capacitor.

**$INTV_{CC}$ (Pin 13):** Internal 5V Regulator Output. The driver and control circuits are powered from this voltage. Bypass this pin to PGND with a minimum 4.7µF ceramic capacitor.

**TG1 (Pin 14):** Top Gate Drive. Drives the top N-channel MOSFET with a voltage equal to $INTV_{CC}$ superimposed on the switch node voltage SW1.

**BST1 (Pin 15):** Bootstrapped Driver Supply. The BST1 pin swings from a diode voltage below $INTV_{CC}$ up to a diode voltage below $V_{IN} + INTV_{CC}$.

**SW1 (Pin 16):** Switch Node. SW1 pin swings from a diode voltage drop below ground up to $V_{IN}$.

**PGND (Pins 17, 20):** Power Ground. Connect these pins closely to the source of the bottom N-channel MOSFET.

**BG1 (Pin 18):** Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and $INTV_{CC}$.

**BG2 (Pin 19):** Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and $INTV_{CC}$.

**SW2 (Pin 21):** Switch Node. SW2 pin swings from a diode voltage drop below ground up to $V_{OUT}$.

# PIN FUNCTIONS

**BST2 (Pin 22):** Bootstrapped Driver Supply. The BST2 pin swings from a diode voltage below INTV$_{CC}$ up to a diode voltage below V$_{OUT}$ + INTV$_{CC}$.

**NC (Pin 23):** No Connect Pin. Leave this pin floating.

**TG2 (Pin 24):** Top Gate Drive. Drives the top N-channel MOSFET with a voltage equal to INTV$_{CC}$ superimposed on the switch node voltage SW2.

**ISP (Pin 25):** Connection Point for the Positive Terminal of the Output Current Feedback Resistor.

**ISN (Pin 26):** Connection Point for the Negative Terminal of the Output Current Feedback Resistor.

**SNSP (Pin 27):** The Positive Input to the Current Sense Comparator. The V$_C$ pin voltage and controlled offsets between the SNSP and SNSN pins, in conjunction with a resistor, set the current trip threshold.

**SNSN (Pin 28):** The Negative Input to the Current Sense Comparator.

**TEST1 (Pin 29):** This pin is used for testing purposes only and must be connected to SGND for the part to operate properly.

**SGND (Pin 30, Exposed Pad Pin 39):** Signal Ground. All small-signal components and compensation should connect to this ground, which should be connected to PGND at a single point. Solder the exposed pad directly to the ground plane.

**PWMOUT (Pin 31):** Buffered Version of PWM Signal for Driving Output Load Disconnect N-Channel MOSFET. The PWMOUT pin is driven from INTV$_{CC}$. Use of a MOSFET with a gate cutoff voltage higher than 1V is recommended.

**CCM (Pin 32):** Continuous Conduction Mode Pin. When the pin voltage is higher than 1.5V, the part runs in fixed frequency forced continuous conduction mode and al-

lows the inductor current to flow negative. When the pin voltage is less than 0.3V, the part runs in discontinuous conduction mode and does not allow the inductor current to flow backward. This pin is only meant to block inductor reverse current, and should only be pulled low when the output current is low. This pin must be either connected to INTV$_{CC}$ (pin 13) for continuous conduction mode across all loads, or it must be connected to the $\overline{C/10}$ (pin 4) with a pull-up resistor to INTV$_{CC}$ for continuous conduction mode at heavy load and for discontinuous conduction mode at light load.

**CLKOUT (Pin 33):** Clock Output Pin. A 180° out-of-phase clock is provided at the oscillator frequency to allow for paralleling two devices for extending output power capability.

**SYNC (Pin 34):** External Synchronization Input Pin. This pin is internally terminated to GND with a 90k resistor. The internal buck clock is synchronized to the rising edge of the SYNC signal while the internal boost clock is 180° phase shifted.

**RT (Pin 35):** Frequency Set Pin. Place a resistor to GND to set the internal frequency. The range of oscillation is 200kHz to 700kHz.

**V$_C$ (Pin 36):** Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0.7V to 1.9V.

**FB (Pin 37):** Voltage Loop Feedback Pin. FB is intended for constant-voltage regulation. The internal transconductance amplifier with output V$_C$ will regulate FB to 1.2V (typical) through the DC/DC converter.

**OVLO (Pin 38):** Overvoltage Input Pin. This pin is used for OVLO, if OVLO > 3V then SS is pulled low, the part stops switching and resets. Do not leave this pin open.

# BLOCK DIAGRAM
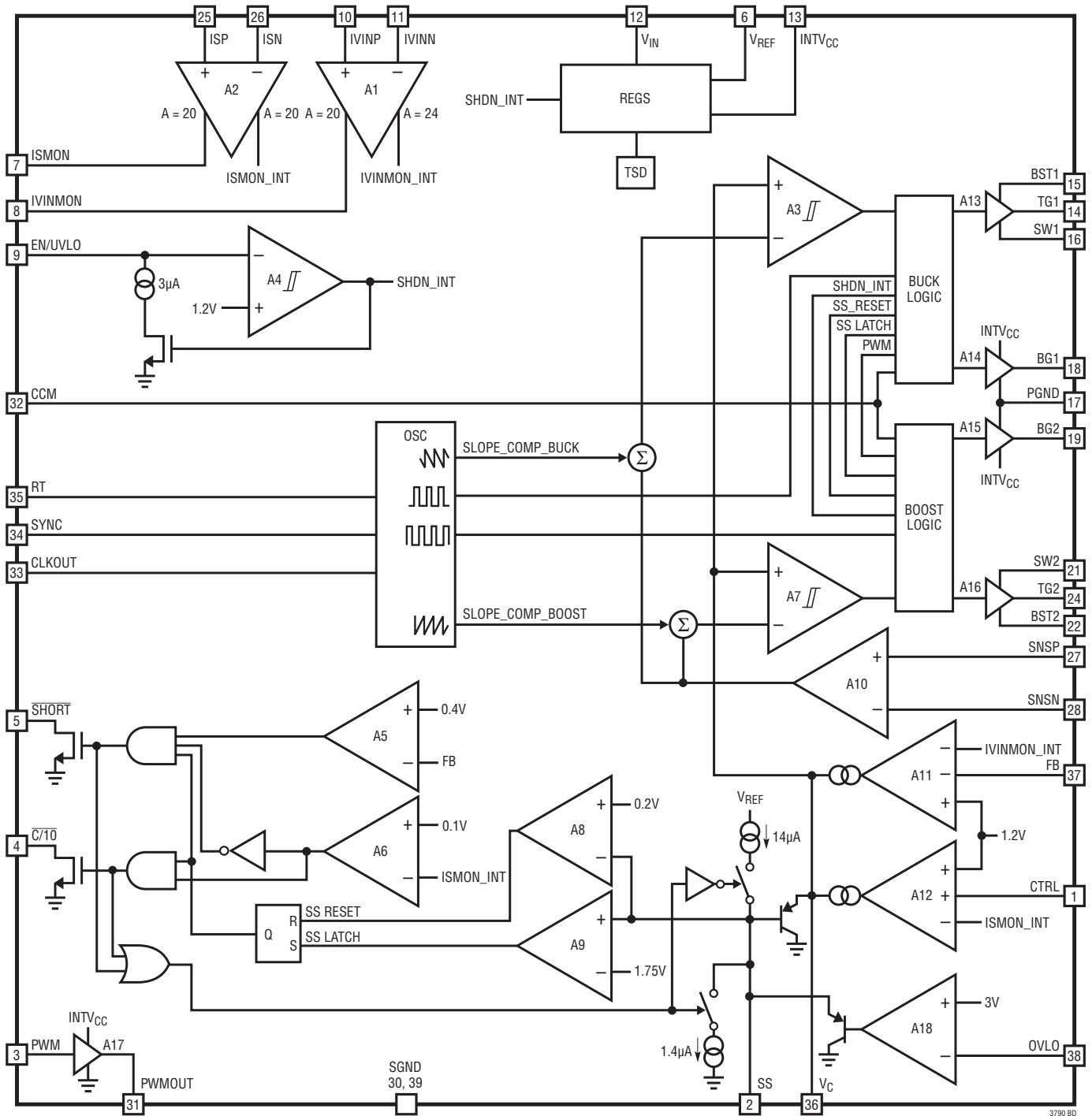
# OPERATION

The LT3790 is a current mode controller that provides an output voltage above, equal to or below the input voltage. The LTC proprietary topology and control architecture uses a current sensing resistor in buck or boost operation. The sensed inductor current is controlled by the voltage on the $V_C$ pin, which is the output of the feedback amplifiers A11 and A12. The $V_C$ pin is controlled by three inputs, one input from the output current loop, one input from the input current loop, and the third input from the feedback loop. Whichever feedback input is higher takes precedence, forcing the converter into either a constant-current or a constant-voltage mode.

The LT3790 is designed to transition cleanly between the two modes of operation. Current sense amplifier A1 senses the voltage between the IVINP and IVINN pins and provides a pre-gain to amplifier A11. When the voltage between IVINP and IVINN reaches 50mV, the output of A1 provides IVINMON_INT to the inverting input of A11 and the converter is in constant-current mode. If the current sense voltage exceeds 50mV, the output of A1 increases causing the output of A11 to decrease, thus reducing the amount of current delivered to the output. In this manner the current sense voltage is regulated to 50mV.

The output current amplifier works similar to the input current amplifier but with a 60mV voltage instead of 50mV. The output current sense level is also adjustable by the CTRL pin. Forcing CTRL to less than 1.2V forces ISMON_INT to the same level as CTRL, thus providing current-level control. The output current amplifier provides rail-to-rail operation. Similarly if the FB pin goes above 1.2V the output of A11 decreases to reduce the current level and regulate the output (constant-voltage mode).

The LT3790 provides monitoring pins IVINMON and ISMON that are proportional to the voltage across the input and output current amplifiers respectively.

The main control loop is shut down by pulling the EN/UVLO pin low. When the EN/UVLO pin is higher than 1.2V, an internal 14µA current source charges soft-start capacitor $C_{SS}$ at the SS pin. The $V_C$ voltage is then clamped a diode voltage higher than the SS voltage while the $C_{SS}$ is slowly charged during start-up. This soft-start clamping prevents abrupt current from being drawn from the input power supply.

The top MOSFET drivers are biased from floating bootstrap capacitors C1 and C2, which are normally recharged through an external diode when the top MOSFET is turned off. A unique charge sharing technique eliminates top FET refresh switching cycle in buck or boost operation. Schottky diodes across the synchronous switch M4 and synchronous switch M2 are not required, but they do provide a lower drop during the dead time. The addition of the Schottky diode typically improves peak efficiency by 1% to 2% at 500kHz.

## Power Switch Control

Figure 1 shows a simplified diagram of how the four power switches are connected to the inductor, $V_{IN}$, $V_{OUT}$ and GND. Figure 2 shows the regions of operation for the LT3790 as a function of duty cycle D. The power switches are properly controlled so the transfer between regions is continuous. When $V_{IN}$ approaches $V_{OUT}$, the buck-boost region is reached.
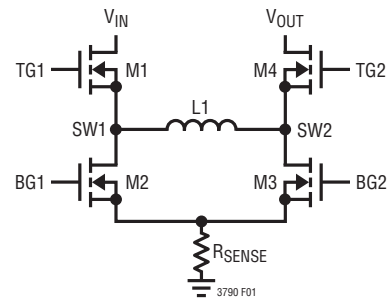


**Figure 1. Simplified Diagram of the Output Switches**



**Figure 2. Operating Regions vs Duty Cycle**

# OPERATION

## Buck Region ($V_{IN} > V_{OUT}$)

Switch M4 is always on and switch M3 is always off during this mode. At the start of every cycle, synchronous switch M2 is turned on first. Inductor current is sensed when synchronous switch M2 is turned on. After the sensed inductor current falls below the reference voltage, which is proportional to $V_C$, synchronous switch M2 is turned off and switch M1 is turned on for the remainder of the cycle. Switches M1 and M2 will alternate, behaving like a typical synchronous buck regulator. The duty cycle of switch M1 increases until the maximum duty cycle of the converter in buck operation reaches $D_{MAX(BUCK, TG1)}$, given by:

$$D_{MAX(BUCK,TG1)} = 100\% - D_{(BUCK-BOOST)}$$

where $D_{(BUCK-BOOST)}$ is the duty cycle of the buck-boost switch range:

$$D_{(BUCK-BOOST)} = 8\%$$

Figure 3 shows typical buck operation waveforms. If $V_{IN}$ approaches $V_{OUT}$, the buck-boost region is reached.

## Buck-Boost Region ($V_{IN} \sim V_{OUT}$)

When $V_{IN}$ is close to $V_{OUT}$, the controller is in buck-boost operation. Figure 4 and Figure 5 show typical waveforms in this operation. Every cycle the controller turns on switches M2 and M4, then M1 and M4 are turned on until 180° later when switches M1 and M3 turn on, and then switches M1 and M4 are turned on for the remainder of the cycle.

## Boost Region ($V_{IN} < V_{OUT}$)

Switch M1 is always on and synchronous switch M2 is always off in boost operation. Every cycle switch M3 is turned on first. Inductor current is sensed when synchronous switch M3 is turned on. After the sensed inductor current exceeds the reference voltage which is proportional to $V_C$, switch M3 turns off and synchronous switch M4 is turned on for the remainder of the cycle. Switches M3 and M4 alternate, behaving like a typical synchronous boost regulator.

The duty cycle of switch M3 decreases until the minimum duty cycle of the converter in boost operation reaches $D_{MIN(BOOST,BG2)}$, given by:

$$D_{MIN(BOOST,BG2)} = D_{(BUCK-BOOST)}$$

where $D_{(BUCK-BOOST)}$ is the duty cycle of the buck-boost switch range:

$$D_{(BUCK-BOOST)} = 8\%$$

Figure 6 shows typical boost operation waveforms. If $V_{IN}$ approaches $V_{OUT}$, the buck-boost region is reached.

## Low Current Operation

The LT3790 is recommended to run in forced continuous conduction mode at heavy load by pulling the CCM pin higher than 1.5V. In this mode the controller behaves as a continuous, PWM current mode synchronous switching regulator. In boost operation, switch M1 is always on, switch M3 and synchronous switch M4 are alternately turned on to maintain the output voltage independent of the direction of inductor current. In buck operation, synchronous switch M4 is always on, switch M1 and synchronous switch M2 are alternately turned on to maintain the output voltage independent of the direction of inductor current. In the forced continuous mode, the output can source or sink current.

However, reverse inductor current from the output to the input is not desired for certain applications. For these applications, the CCM pin must be connected to $\overline{C/10}$ (pin 4) with a pull-up resistor to $INTV_{CC}$ (see front page Typical Application). Therefore, the CCM pin will be pulled lower than 0.3V for discontinuous conduction mode by the $\overline{C/10}$ pin when the output current is low. In this mode, switch M4 turns off when the inductor current flows negative.
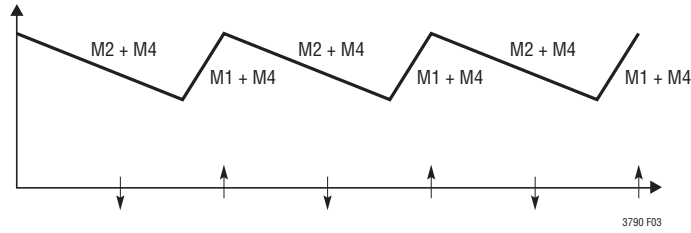
# OPERATION
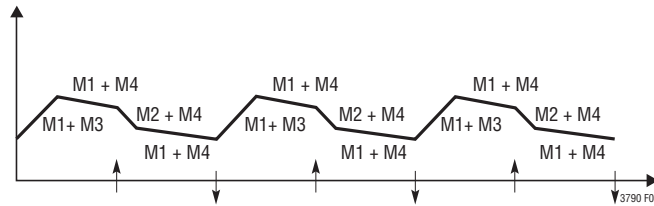
Figure 3. Buck Operation ($V_{IN} > V_{OUT}$)

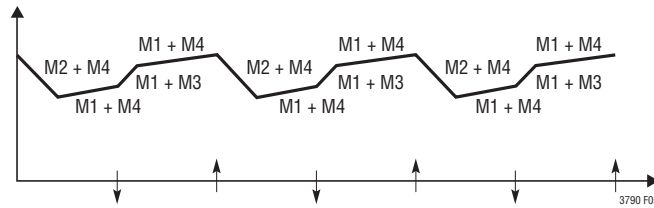Figure 4. Buck-Boost Operation ($V_{IN} \leq V_{OUT}$)

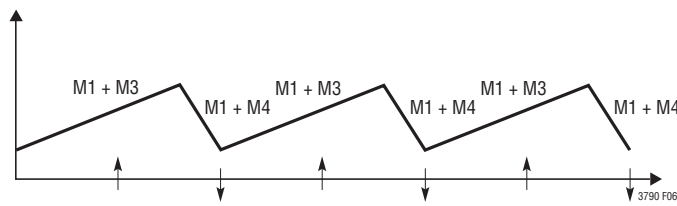Figure 5. Buck-Boost Operation ($V_{IN} \geq V_{OUT}$)

Figure 6. Boost Operation ($V_{IN} < V_{OUT}$)

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# APPLICATIONS INFORMATION

The Typical Application on the front page is a basic LT3790 application circuit. External component selection is driven by the load requirement, and begins with the selection of $R_{SENSE}$ and the inductor value. Next, the power MOSFETs are selected. Finally, $C_{IN}$ and $C_{OUT}$ are selected. This circuit can operate up to an input voltage of 60V.

## Programming The Switching Frequency

The RT frequency adjust pin allows the user to program the switching frequency from 200kHz to 700kHz to optimize efficiency/performance or external component size. Higher frequency operation yields smaller component size but increases switching losses and gate driving current, and may not allow sufficiently high or low duty cycle operation. Lower frequency operation gives better performance at the cost of larger external component size. For an appropriate $R_T$ resistor value see Table 1. An external resistor from the RT pin to GND is required; do not leave this pin open.

**Table 1. Switching Frequency vs $R_T$ Value**

| $f_{OSC}$ (kHz) | $R_T$ (kΩ) |
|---|---|
| 200 | 147 |
| 300 | 84.5 |
| 400 | 59.0 |
| 500 | 45.3 |
| 600 | 35.7 |
| 700 | 29.4 |

## Frequency Synchronization

The LT3790 switching frequency can be synchronized to an external clock using the SYNC pin. Driving SYNC with a 50% duty cycle waveform is always a good choice, otherwise maintain the duty cycle between 10% and 90%. The falling edge of CLKOUT corresponds to the rising edge of SYNC thus allowing 2-phase paralleling converters. The rising edge of CLKOUT turns on switch M3 and the falling edge of CLKOUT turns on switch M2.

## Inductor Selection

The operating frequency and inductor selection are inter-related in that higher operating frequencies allow the use of smaller inductor and capacitor values. The inductor
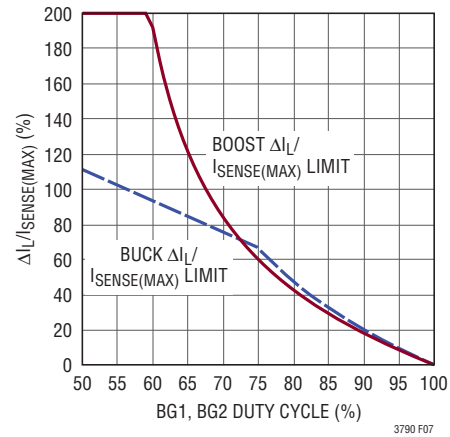


**Figure 7. Maximum Peak-to-Peak Ripple vs Duty Cycle**

value has a direct effect on ripple current. The maximum inductor current ripple $\Delta I_L$ can be seen in Figure 7. This is the maximum ripple that will prevent subharmonic oscillation and also regulate with zero load. The ripple should be less than this to allow proper operation over all load currents. For a given ripple the inductance terms in continuous mode are as follows:

$$L_{BUCK} > \frac{V_{OUT} \cdot \left( V_{IN(MAX)} - V_{OUT} \right) \cdot 100}{f \cdot I_{OUT(MAX)} \cdot \%Ripple \cdot V_{IN(MAX)}}$$

$$L_{BOOST} > \frac{V_{IN(MIN)}^2 \cdot \left( V_{OUT} - V_{IN(MIN)} \right) \cdot 100}{f \cdot I_{OUT(MAX)} \cdot \%Ripple \cdot V_{OUT}^2}$$

where:

f is operating frequency

% ripple is allowable inductor current ripple

$V_{IN(MIN)}$ is minimum input voltage

$V_{IN(MAX)}$ is maximum input voltage

$V_{OUT}$ is output voltage

$I_{OUT(MAX)}$ is maximum output load current

For high efficiency, choose an inductor with low core loss. Also, the inductor should have low DC resistance to reduce the $I^2R$ losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor.

# APPLICATIONS INFORMATION

## R$_{SENSE}$ Selection and Maximum Output Current

R$_{SENSE}$ is chosen based on the required output current. The current comparator threshold sets the peak of the inductor current in boost operation and the maximum inductor valley current in buck operation. In boost operation, the maximum average load current at V$_{IN(MIN)}$ is:

$$I_{OUT(MAX\_BOOST)} = \left( \frac{51mV}{R_{SENSE}} - \frac{\Delta I_L}{2} \right) \bullet \frac{V_{IN(MIN)}}{V_{OUT}}$$

where $\Delta I_L$ is peak-to-peak inductor ripple current. In buck operation, the maximum average load current is:

$$I_{OUT(MAX\_BUCK)} = \left( \frac{47.5mV}{R_{SENSE}} + \frac{\Delta I_L}{2} \right)$$

The maximum current sensing R$_{SENSE}$ value for the boost operation is:

$$R_{SENSE(MAX)} = \frac{2 \bullet 51mV \bullet V_{IN(MIN)}}{2 \bullet I_{OUT} \bullet V_{OUT} + \Delta I_{L(BOOST)} \bullet V_{IN(MIN)}}$$

The maximum current sensing R$_{SENSE}$ value for the buck operation is:

$$R_{SENSE(MAX)} = \frac{2 \bullet 47.5mV}{2 \bullet I_{OUT} - \Delta I_{L(BUCK)}}$$

The final R$_{SENSE}$ value should be lower than the calculated R$_{SENSE(MAX)}$ in both the boost and buck operation. A 20% to 30% margin is usually recommended.

## C$_{IN}$ and C$_{OUT}$ Selection

In boost operation, input current is continuous. In buck operation, input current is discontinuous. In buck operation, the selection of input capacitor, C$_{IN}$, is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current. For buck operation, the input RMS current is given by:

$$I_{RMS} = \sqrt{I_{OUT}^2 \bullet D + \frac{\Delta I_L^2}{12} \bullet D}$$

The formula has a maximum at V$_{IN}$ = 2V$_{OUT}$. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor.

In boost operation, the discontinuous current shifts from the input to the output, so C$_{OUT}$ must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{RIPPLE\ (BOOST\_CAP)} = \frac{I_{OUT} \bullet \left( V_{OUT} - V_{IN(MIN)} \right)}{C_{OUT} \bullet V_{OUT} \bullet f}$$

$$\Delta V_{RIPPLE\ (BUCK\_CAP)} \approx \frac{\Delta I_L}{8 \bullet f \bullet C_{OUT}}$$

where C$_{OUT}$ is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{BOOST(ESR)} = I_{OUT} \bullet ESR$$

$$\Delta V_{BUCK(ESR)} = I_{OUT} \bullet ESR$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Output capacitors are also used for stability for the LT3790. A good starting point for output capacitors is seen in the Typical Applications circuits. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and are recommended for applications less than 100W. Capacitors available with low ESR and high ripple current ratings, such as OS-CON and POSCAP may be needed for applications greater than 100W.

# APPLICATIONS INFORMATION

## Programming $V_{IN}$ UVLO and OVLO

The falling UVLO value can be accurately set by the resistor divider R1 and R2. A small 3µA pull-down current is active when the EN/UVLO is below the threshold. The purpose of this current is to allow the user to program the rising hysteresis. The following equations should be used to determine the resistor values:

$$V_{IN(UVLO^-)} = 1.2 \bullet \frac{R1+R2}{R2}$$

$$V_{IN(UVLO^+)} = 3\mu A \bullet R1 + 1.215 \bullet \frac{R1+R2}{R2}$$

The rising OVLO value can be accurately set by the resistor divider R3 and R4. The following equations should be used to determine the resistor values:

$$V_{IN(OVLO^+)} = 3 \bullet \frac{R3+R4}{R4}$$

$$V_{IN(OVLO^-)} = 2.925 \bullet \frac{R3+R4}{R4}$$
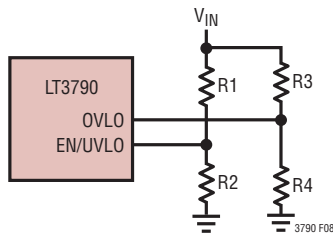


**Figure 8. Resistor Connection to Set $V_{IN}$ UVLO and OVLO Thresholds**

## Programming Output Current

The output current is programmed by placing an appropriate value current sense resistor, $R_{OUT}$, in series with the output load. The voltage drop across $R_{OUT}$ is (Kelvin) sensed by the ISP and ISN pins. The CTRL pin should be tied to a voltage higher than 1.2V to get the full-scale 60mV (typical) threshold across the sense resistor. The CTRL pin can also be used to adjust the output current, although relative accuracy decreases with the decreasing sense threshold. When the CTRL pin voltage is less than 1.1V, the output current is:

$$I_{OUT} = \frac{V_{CTRL}}{R_{OUT} \bullet 20}$$

When the CTRL pin voltage is between 1.1V and 1.3V the output current varies with $V_{CTRL}$, but departs from the equation above by an increasing amount as $V_{CTRL}$ voltage increases. Ultimately, when $V_{CTRL} > 1.3V$ the output current no longer varies. The typical $V_{(ISP-ISN)}$ threshold vs $V_{CTRL}$ is listed in Table 2.

**Table 2. $V_{(ISP-ISN)}$ Threshold vs CTRL**

| $V_{CTRL}$ (V) | $V_{(ISP-ISN)}$ (mV) |
|---|---|
| 1.1 | 54.6 |
| 1.15 | 57 |
| 1.2 | 58.8 |
| 1.25 | 59.7 |
| 1.3 | 60 |

When $V_{CTRL}$ is higher than 1.3V, the output current is regulated to:

$$I_{OUT} = \frac{60mV}{R_{OUT}}$$

The CTRL pin should not be left open (tie to $V_{REF}$ if not used). The CTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the output load, or with a resistor divider to $V_{IN}$ to reduce output power and switching current when $V_{IN}$ is low. The presence of a time varying differential voltage signal (ripple) across ISP and ISN at the switching frequency is expected. The amplitude of this signal is increased by high output load current, low switching frequency and/or a smaller value output filter capacitor. Some level of ripple signal is acceptable: the compensation capacitor on the $V_C$ pin filters the signal so the average difference between ISP and ISN is regulated to the user-programmed value. Ripple voltage amplitude (peak-to-peak) in excess of 20mV should not cause mis-operation, but may lead to noticeable offset between the average value and the user-programmed value.

### ISMON

The ISMON pin provides a linear indication of the current flowing through the output. The equation for $V_{ISMON}$ is $V_{(ISP-ISN)} \bullet 20$. This pin is suitable for driving an ADC input, however, the output impedance of this pin is 12.5kΩ so care must be taken not to load this pin.

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# APPLICATIONS INFORMATION

## Programming Input Current Limit

The LT3790 has a standalone current sense amplifier. It can be used to limit the input current. The input current limit is calculated by the following equation:

$$I_{IN} = \frac{50mV}{R_{IN}}$$

For loop stability a lowpass RC filter is needed. For most applications, a 50Ω resistor and 470nF capacitor is sufficient.

**Table 3**

| $R_{IN}$ (mΩ) | $I_{LIMIT}$ (A) |
|---|---|
| 20 | 2.5 |
| 15 | 3.3 |
| 12 | 4.2 |
| 10 | 5.0 |
| 6 | 8.3 |
| 5 | 10.0 |
| 4 | 12.5 |
| 3 | 16.7 |
| 2 | 25 |

## IVINMON

The IVINMON pin provides a linear indication of the current flowing through the input. The equation for $V_{IVINMON}$ is $V_{(IVINP-IVINN)} \cdot 20$. This pin is suitable for driving an ADC input, however, the output impedance of this pin is 12.5kΩ so care must be taken not to load this pin.

## Programming Output Voltage (Constant Voltage Regulation)

For a voltage regulator, the output voltage can be set by selecting the values of R5 and R6 (see Figure 9) according to the following equation:

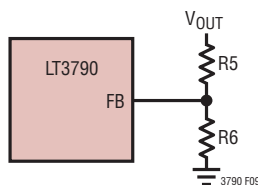$$V_{OUT} = 1.2 \cdot \frac{R5 + R6}{R6}$$



**Figure 9. Resistor Connection for Constant Output Voltage Regulation**

## Dimming Control

There are two methods to control the current source for dimming using the LT3790. One method uses the CTRL pin to adjust the current regulated in the output. A second method uses the PWM pin to modulate the current source between zero and full current to achieve a precisely programmed average current. To make PWM dimming more accurate, the switch demand current is stored on the $V_C$ node during the quiescent phase when PWM is low. This feature minimizes recovery time when the PWM signal goes high. To further improve the recovery time a disconnect switch may be used in the output current path to prevent the ISP node from discharging during the PWM signal low phase. The minimum PWM on- or off-time is affected by choice of operating frequency and external component selection. The best overall combination of PWM and analog dimming capabilities is available if the minimum PWM pulse is at least six switching cycles and the PWM pulse is synchronized to the SYNC signal.

## $\overline{SHORT}$ Pin

The LT3790 provides an open-drain status pin, $\overline{SHORT}$, which pulls low when the FB pin is below 400mV and $V_{(ISP-ISN)}$ is above 5mV. The only time the FB pin will be below 400mV is during start-up or if the output is shorted. During start-up the LT3790 ignores the voltage on the FB pin until the soft-start capacitor reaches 1.75V. To prevent false tripping after startup, a large enough soft-start capacitor must be used to allow the output to get up to approximately 40% to 50% of the final value.

## $\overline{C/10}$ Pin

The LT3790 provides an open-drain status pin, $\overline{C/10}$, which pulls low when the voltage across $V_{(ISP-ISN)}$ is less than 5mV. For battery charger applications with output current sense and limit, the $\overline{C/10}$ provides a C/10 charge termination flag.

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# APPLICATIONS INFORMATION

## Soft-Start

Soft-start reduces the input power sources' surge currents by gradually increasing the controller's current limit (proportional to an internally buffered clamped equivalent of $V_C$). The soft-start interval is set by the soft-start capacitor selection according to the following equation

$$t_{SS} = \frac{1.2V}{14\mu A} \bullet C_{SS}$$

A 100k resistor must be placed between SS and $V_{REF}$ for the LT3790. This 100k resistor also contributes the extra SS charge current. Make sure $C_{SS}$ is large enough when there is loading during start-up.

## Loop Compensation

The LT3790 uses an internal transconductance error amplifier whose $V_C$ output compensates the control loop. The external inductor, output capacitor and the compensation resistor and capacitor determine the loop stability.

The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor at $V_C$ are set to optimize control loop response and stability. For typical applications, a 22nF or higher compensation capacitor at $V_C$ is needed, and a series resistor should always be used to increase the slew rate on the $V_C$ pin to maintain tighter regulation of output current during fast transients on the input supply of the converter.

## Power MOSFET Selections and Efficiency Considerations

The LT3790 requires four external N-channel power MOSFETs, two for the top switches (switch M1 and M4, shown in Figure 1) and two for the bottom switches (switch M2 and M3 shown in Figure 1). Important parameters for the power MOSFETs are the breakdown voltage, $V_{BR(DSS)}$, threshold voltage, $V_{GS(TH)}$, on-resistance, $R_{DS(ON)}$, reverse transfer capacitance, $C_{RSS}$, and maximum current, $I_{DS(MAX)}$.

The drive voltage is set by the 5V $INTV_{CC}$ supply. Consequently, logic-level threshold MOSFETs must be used in LT3790 applications. If the input voltage is expected to drop below the 5V, then sub-logic threshold MOSFETs should be considered.

In order to select the power MOSFETs, the power dissipated by the device must be known. For switch M1, the maximum power dissipation happens in boost operation, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$P_{M1(BOOST)} = \left( \frac{I_{OUT} \bullet V_{OUT}}{V_{IN}} \right)^2 \bullet \rho_T \bullet R_{DS(ON)}$$

where $\rho_T$ is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically 0.4%/°C as shown in Figure 10. For a maximum junction temperature of 125°C, using a value of $\rho_T = 1.5$ is reasonable.

Switch M2 operates in buck operation as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$P_{M2(BUCK)} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

Switch M3 operates in boost operation as the control switch. Its power dissipation at maximum current is given by:

$$P_{M3(BOOST)} = \frac{(V_{OUT} - V_{IN}) \bullet V_{OUT}}{V_{IN}^2} \bullet I_{OUT}^2 \bullet \rho_T \bullet R_{DS(ON)}$$
$$+ k \bullet V_{OUT}^3 \bullet \frac{I_{OUT}}{V_{IN}} \bullet C_{RSS} \bullet f$$

where $C_{RSS}$ is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused by reverse-recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch M4, the maximum power dissipation happens in boost operation, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{M4(BOOST)} = \frac{V_{IN}}{V_{OUT}} \bullet \left( \frac{I_{OUT} \bullet V_{OUT}}{V_{IN}} \right)^2 \bullet \rho_T \bullet R_{DS(ON)}$$

For the same output voltage and current, switch M1 has the highest power dissipation and switch M2 has the lowest power dissipation unless a short occurs at the output.

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# APPLICATIONS INFORMATION

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \cdot R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in the equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(JC)}$). This value of $T_J$ can then be compared to the original, assumed value used in the iterative calculation process.
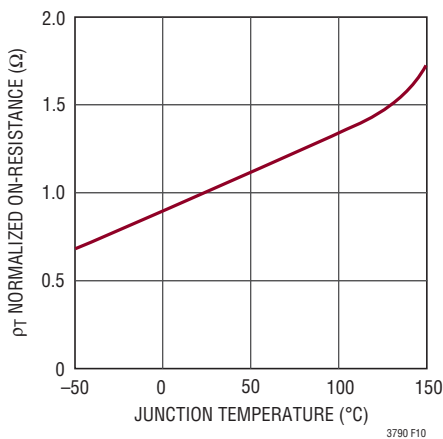


**Figure 10. Normalized $R_{DS(ON)}$ vs Temperature**

### Optional Schottky Diode (D3, D4) Selection

The Schottky diodes D3 and D4 shown in the Typical Applications section conduct during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diode of synchronous switches M2 and M4 from turning on and storing charge during the dead time. In particular, D4 significantly reduces reverse-recovery current between switch M4 turn-off and switch M3 turn-on, which improves converter efficiency and reduces switch M3 voltage stress. In order for the diode to be effective, the inductance between it and the synchronous switch must be as small as possible, mandating that these components be placed adjacently.

### INTV$_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5V at the INTV$_{CC}$ pin from the V$_{IN}$ supply pin. INTV$_{CC}$ powers the drivers and internal circuitry within the LT3790. The

INTV$_{CC}$ pin regulator can supply a peak current of 67mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. An additional 0.1µF ceramic capacitor placed directly adjacent to the INTV$_{CC}$ and PGND IC pins is highly recommended. Good bypassing is necessary to supply the high transient current required by MOSFET gate drivers.

Higher input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LT3790 to be exceeded. The system supply current is normally dominated by the gate charge current. Additional external loading of the INTV$_{CC}$ also needs to be taken into account for the power dissipation calculations. Power dissipation for the IC in this case is V$_{IN}$ • I$_{INTVCC}$, and overall efficiency is lowered. The junction temperature can be estimated by using the equations given

$$T_J = T_A + (P_D \cdot \theta_{JA})$$

where $\theta_{JA}$ (in °C/W) is the package thermal impedance.

For example, a typical application operating in continuous current operation might draw 24mA from a 24V supply:

$$T_J = 70°C + 24mA \cdot 24V \cdot 28°C/W = 86°C$$

To prevent maximum junction temperature from being exceeded, the input supply current must be checked operating in continuous mode at maximum V$_{IN}$.

### Top Gate (TG) MOSFET Driver Supply (C1, D1, C2, D2)

The external bootstrap capacitors C1 and C2 connected to the BST1 and BST2 pins supply the gate drive voltage for the topside MOSFET switches M1 and M4. When the top MOSFET switch M1 turns on, the switch node SW1 rises to V$_{IN}$ and the BST1 pin rises to approximately V$_{IN}$ + INTV$_{CC}$. When the bottom MOSFET switch M2 turns on, the switch node SW1 drops low and the bootstrap capacitor C1 is charged through D1 from INTV$_{CC}$. When the bottom MOSFET switch M3 turns on, the switch node SW2 drops low and the bootstrap capacitor C2, is charged through D2 from INTV$_{CC}$. The bootstrap capacitors C1 and C2 need to store about 100 times the gate charge required by the top MOSFET switch M1 and M4. In most applications a 0.1µF to 0.47µF, X5R or X7R ceramic capacitor is adequate.

# APPLICATIONS INFORMATION

## Efficiency Considerations

The power efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in circuits produce losses, four main sources account for most of the losses in LT3790 circuits:

1. DC $I^2R$ losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.

2. Transition loss. This loss arises from the brief amount of time switch M1 or switch M3 spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V and can be estimated from:

   $$\text{Transition Loss} \approx 2.7 \cdot V_{IN}^2 \cdot I_{OUT} \cdot C_{RSS} \cdot f$$

   where $C_{RSS}$ is the reverse-transfer capacitance.

3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents.

4. $C_{IN}$ and $C_{OUT}$ loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck operation. The output capacitor has the difficult job of filtering the large RMS output current in boost operation. Both $C_{IN}$ and $C_{OUT}$ are required to have low ESR to minimize the AC $I^2R$ loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

5. Other losses. Schottky diode D3 and D4 are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss occurs predominately at light loads. Switch M3 causes reverse recovery current loss in boost operation.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in the input current, then there is no change in efficiency.

## PC Board Layout Checklist

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

- The PGND ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.

- Place $C_{IN}$, switch M1, switch M2 and D1 in one compact area. Place $C_{OUT}$, switch M3, switch M4 and D2 in one compact area.

- Use immediate vias to connect the components (including the LT3790's SGND and PGND pins) to the ground plane. Use several large vias for each power component.

- Use planes for $V_{IN}$ and $V_{OUT}$ to maintain good voltage filtering and to keep power losses low.

- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net ($V_{IN}$ or PGND).

- Separate the signal and power grounds. All small-signal components should return to the SGND pin at one point, which is then tied to the PGND pin close to the sources of switch M2 and switch M3.

- Place switch M2 and switch M3 as close to the controller as possible, keeping the PGND, BG and SW traces short.

- Keep the high dV/dT SW1, SW2, BST1, BST2, TG1 and TG2 nodes away from sensitive small-signal nodes.

- The path formed by switch M1, switch M2, D1 and the $C_{IN}$ capacitor should have short leads and PC trace lengths. The path formed by switch M3, switch M4, D2 and the $C_{OUT}$ capacitor also should have short leads and PC trace lengths.

- The output capacitor (−) terminals should be connected as close as possible to the (−) terminals of the input capacitor.

- Connect the top driver bootstrap capacitor, C1, closely to the BST1 and SW1 pins. Connect the top driver bootstrap capacitor, C2, closely to the BST2 and SW2 pins.

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# APPLICATIONS INFORMATION

■ Connect the input capacitors, $C_{IN}$, and output capacitors, $C_{OUT}$, closely to the power MOSFETs. These capacitors carry the MOSFET AC current in boost and buck operation.

■ Route SNSN and SNSP leads together with minimum PC trace spacing. Avoid sense lines pass through noisy areas, such as switch nodes. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.

■ Connect the $V_C$ pin compensation network close to the IC, between $V_C$ and the signal ground pins. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.

■ Connect the $INTV_{CC}$ bypass capacitor, $C_{VCC}$, close to the IC, between the $INTV_{CC}$ and the power ground pins. This capacitor carries the MOSFET drivers' current peaks. An additional 0.1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.
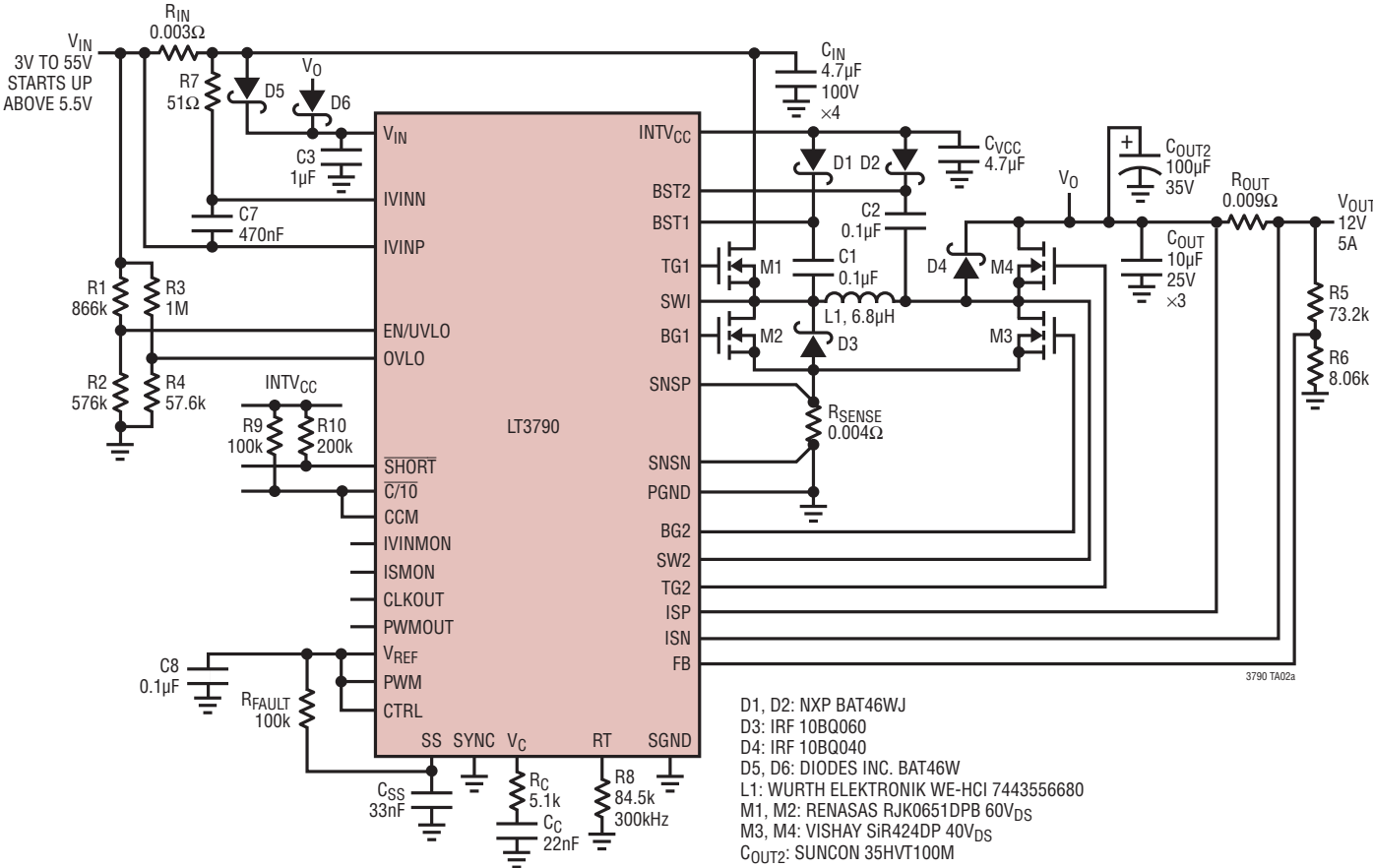
**Differences Between LT3790 and LT3791-1**

The LT3790 is an improved version of the LT3791-1 and is recommended for use in new designs. Some external component values may change, but otherwise, the LT3790 is functionally equivalent to the LT3791-1. The differences between the two products are:
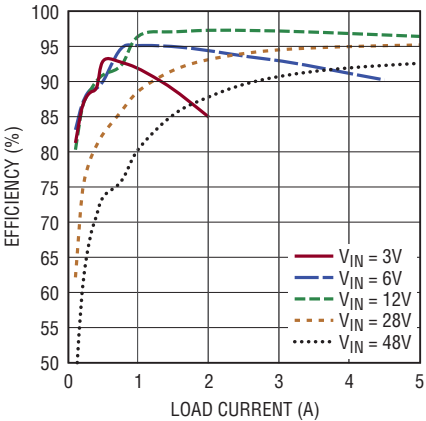
1. The LT3790 has a 60mV (typical) full-scale $V_{(ISP-ISN)}$ current sense voltage, compared to 100mV (typical) for the LT3791-1. This change allows lower power current sense resistors to be used for most applications.

2. The LT3790 CTRL pin linear range is from 0V to 1.1V, and has a turn-off threshold of 50mV (typical), compared to a 200mV to 1.1V linear range and 175mV (typical) turn-off threshold for the LT3791-1. These changes make it easier to parallel two or more LT3790 ICs for higher power levels.

3. The LT3790 $\overline{C/10}$ pin pulls low when the $V_{(ISP-ISN)}$ voltage is less than 1/10 full scale, compared to the LT3791-1, where $\overline{C/10}$ pulls low when both $V_{(ISP-ISN)}$ is less than 1/10 full scale and $V_{FB}$ is greater than 1.15V (typical). Since the $\overline{C/10}$ pin is used to allow DCM mode for some applications, this change ensures that negative current does not occur at light loads for a broader range of applications.

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# TYPICAL APPLICATIONS

### 98% Efficient 60W (12V 5A) Voltage Regulator Runs Down to 3V $V_{IN}$



D1, D2: NXP BAT46WJ
D3: IRF 10BQ060
D4: IRF 10BQ040
D5, D6: DIODES INC. BAT46W
L1: WURTH ELEKTRONIK WE-HCI 7443556680
M1, M2: RENASAS RJK0651DPB 60$V_{DS}$
M3, M4: VISHAY SiR424DP 40$V_{DS}$
$C_{OUT2}$: SUNCON 35HVT100M

3790 TA02a

**Efficiency vs Load Current**



3790 TA02b

**Maximum Output Current vs $V_{IN}$**



3790 TA02c
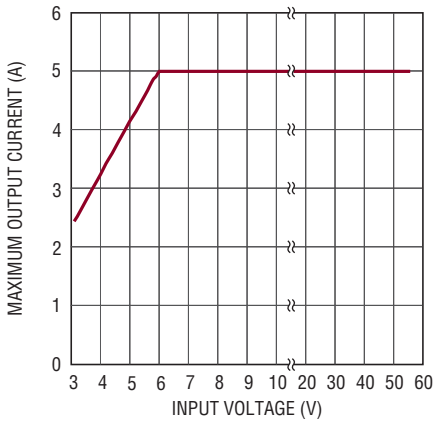
# TYPICAL APPLICATIONS

**98% Efficient 240W (24V 10A) Parallel Voltage Regulators**



**Transient Waveform**

V$_{IN}$ = 36V
I$_{OUT}$ = 5A TO 10A

**Startup Waveform**

V$_{IN}$ = 36V
I$_{OUT}$ = 5A
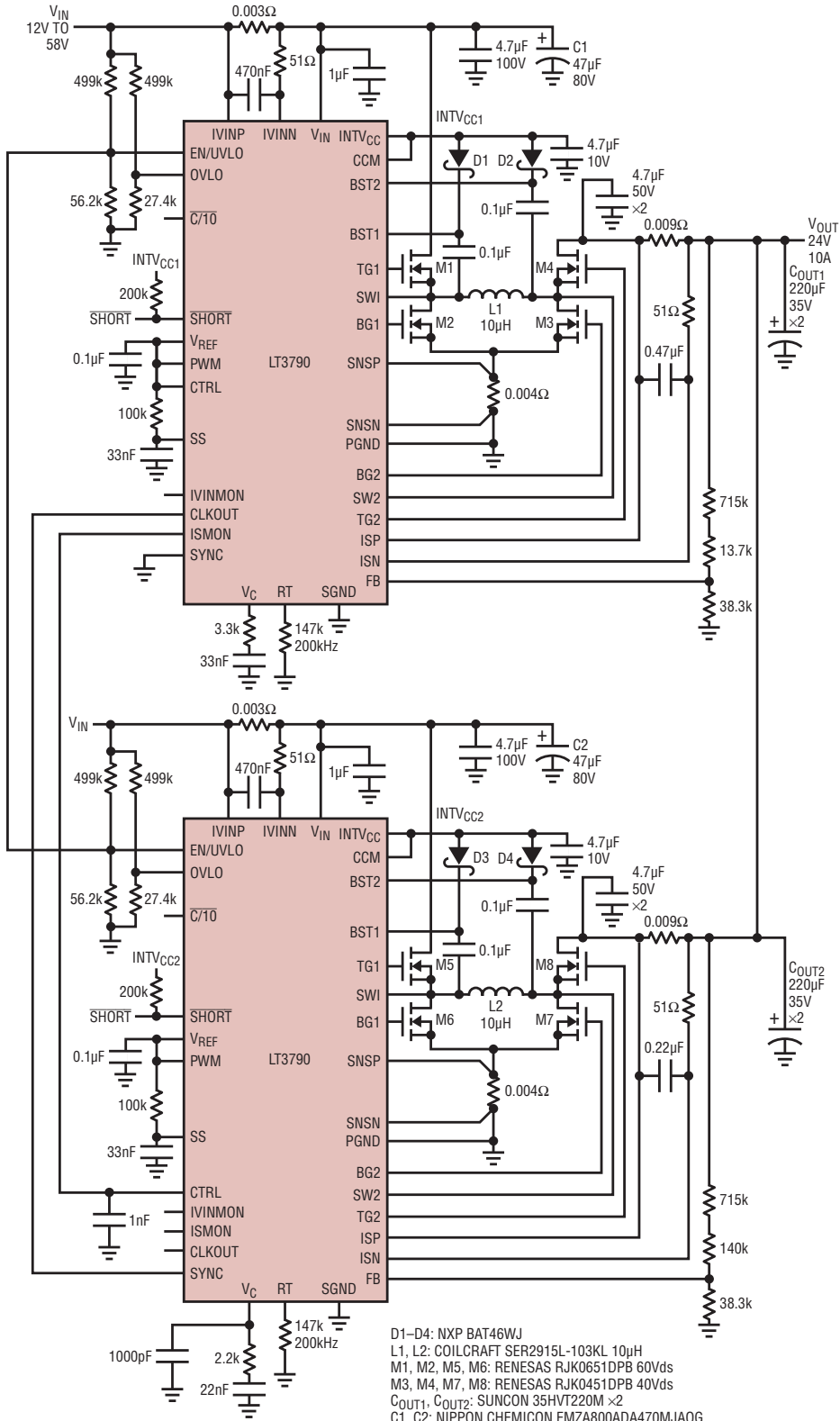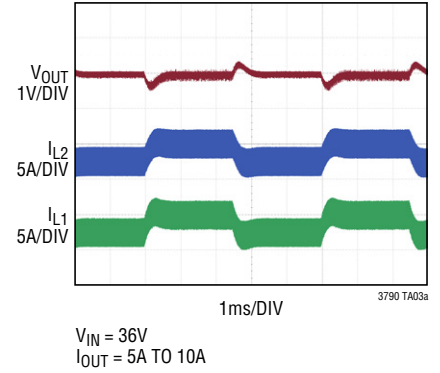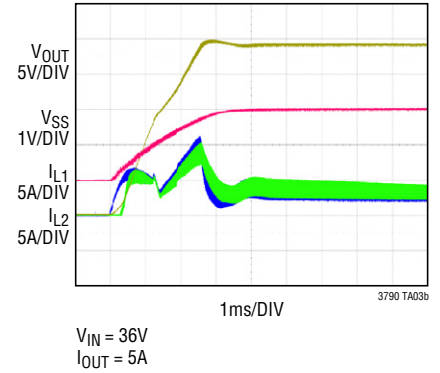
**Mismatch Current vs Load Current**

D1–D4: NXP BAT46WJ
L1, L2: COILCRAFT SER2915L-103KL 10µH
M1, M2, M5, M6: RENESAS RJK0651DPB 60Vds
M3, M4, M7, M8: RENESAS RJK0451DPB 40Vds
C$_{OUT1}$, C$_{OUT2}$: SUNCON 35HVT220M ×2
C1, C2: NIPPON CHEMICON EMZA800ADA470MJAOG

3790 TA03
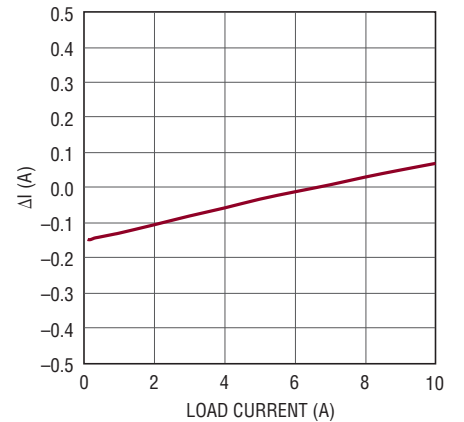
# TYPICAL APPLICATIONS

### 98% Efficient 360W (24V 15A) Parallel Voltage Regulators



D1–D4: NXP BAT46WJ
L1, L2: COILCRAFT SER2915L-103KL 10µH
M1, M2, M5, M6: RENESAS RJK0651DPB 60Vds
M3, M4, M7, M8: RENESAS RJK0451DPB 40Vds
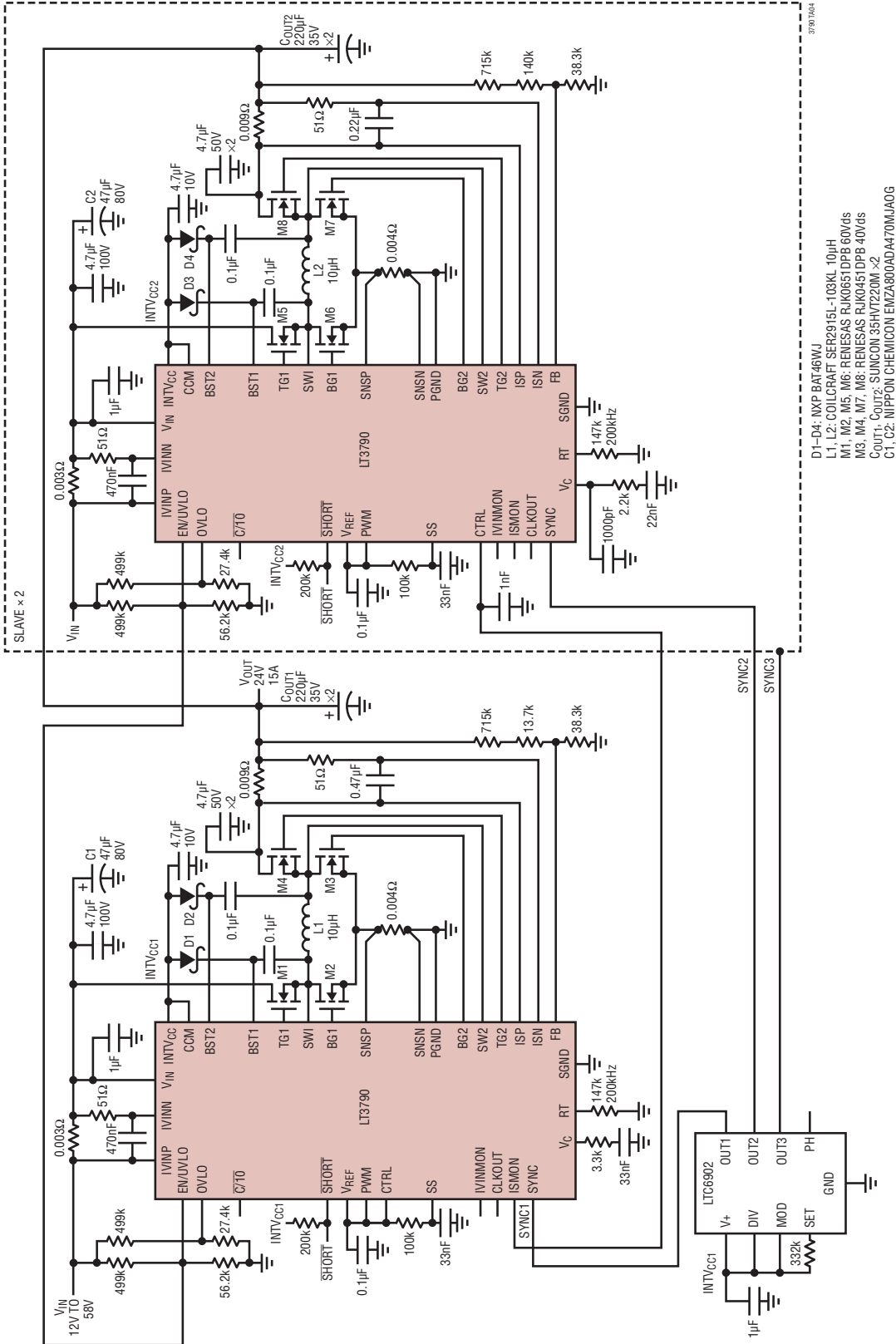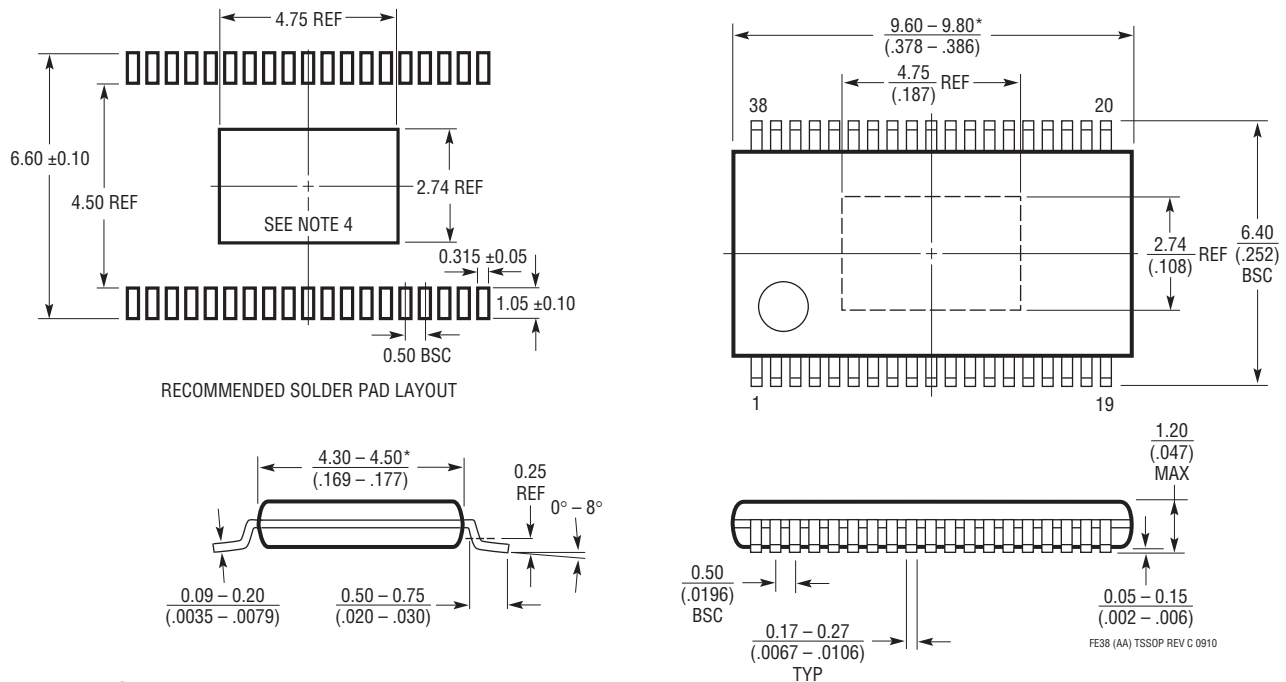C$_{OUT1}$, C$_{OUT2}$: SUNCON 35HVT220M ×2
C1, C2: NIPPON CHEMICON EMZA800ADA470MJA0G

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LT3790#packaging for the most recent package drawings.**

**FE Package**
**38-Lead Plastic TSSOP (4.4mm)**
(Reference LTC DWG # 05-08-1772 Rev C)
**Exposed Pad Variation AA**

4.75 REF

6.60 ±0.10

4.50 REF

2.74 REF

SEE NOTE 4

0.315 ±0.05

1.05 ±0.10

0.50 BSC

RECOMMENDED SOLDER PAD LAYOUT

9.60 – 9.80*
(.378 – .386)

$\frac{4.75}{(.187)}$ REF

38

20

$\frac{2.74}{(.108)}$ REF

$\frac{6.40}{(.252)}$ BSC

1

19

$\frac{4.30 - 4.50*}{(.169 - .177)}$

0.25 REF

0° – 8°

$\frac{0.09 - 0.20}{(.0035 - .0079)}$

$\frac{0.50 - 0.75}{(.020 - .030)}$

$\frac{1.20}{(.047)}$ MAX

$\frac{0.50}{(.0196)}$ BSC

$\frac{0.17 - 0.27}{(.0067 - .0106)}$ TYP

$\frac{0.05 - 0.15}{(.002 - .006)}$

FE38 (AA) TSSOP REV C 0910

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS
   (INCHES)
3. DRAWING NOT TO SCALE

4. RECOMMENDED MINIMUM PCB METAL SIZE
   FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH
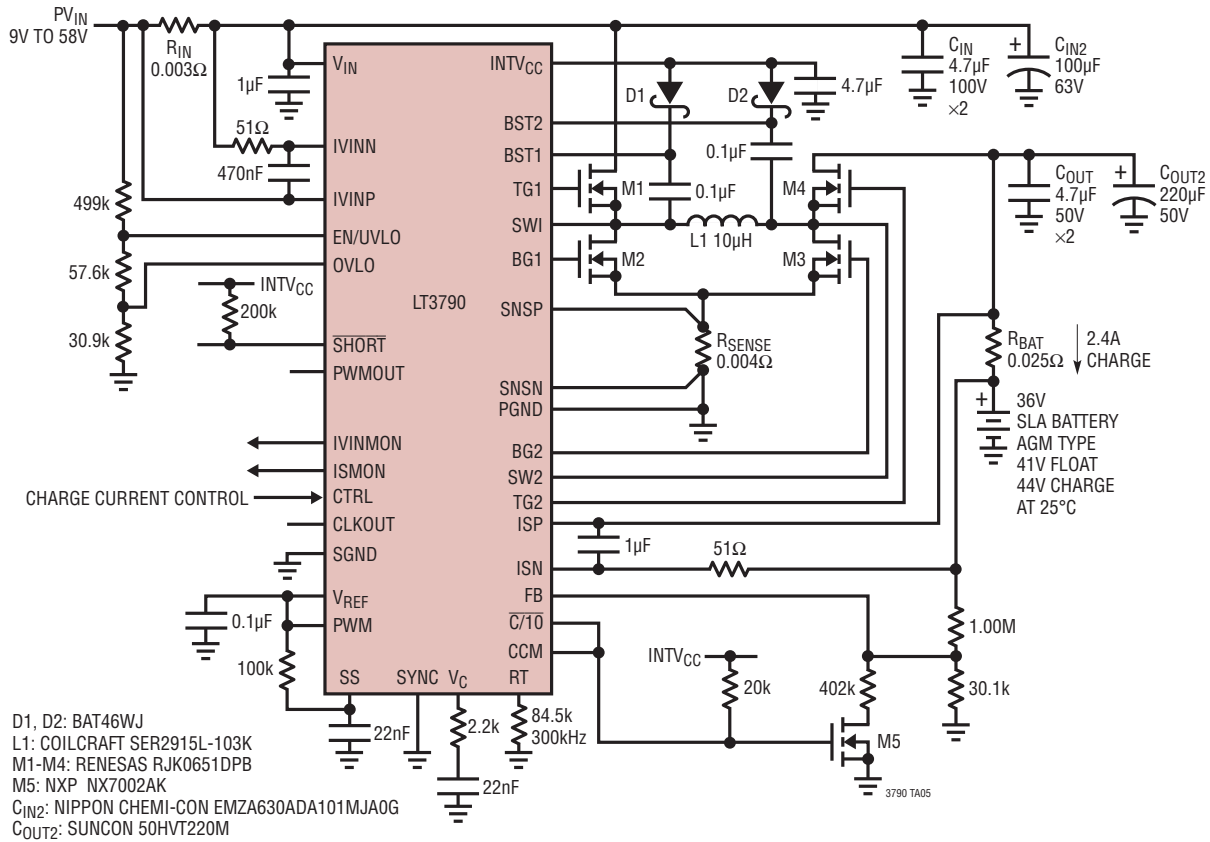 SHALL NOT EXCEED 0.150mm (.006") PER SIDE

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# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|-----|------|-------------|-------------|
| A | 12/15 | Clarified Typical Application schematic | 1 |
| | | Clarified Electrical $V_{(ISP-ISN)}$ Threshold parameters | 3 |
| | | Clarified ISP/ISN Bias Current parameters | 3 |
| | | Clarified Block Diagram | 11 |
| | | Clarified $I_{LED}$ to $I_{OUT}$ in Equations | 17, 20 |
| | | Clarified Loop Compensation paragraph | 10 |

# TYPICAL APPLICATION

**2.4A Buck-Boost 36V SLA Battery Charger**



D1, D2: BAT46WJ
L1: COILCRAFT SER2915L-103K
M1-M4: RENESAS RJK0651DPB
M5: NXP NX7002AK
C_IN2: NIPPON CHEMI-CON EMZA630ADA101MJA0G
C_OUT2: SUNCON 50HVT220M

# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LT3791 | 60V 4-Switch Synchronous Buck-Boost LED Driver | $4.7V \leq V_{IN} \leq 60V$, $1.2V \leq V_{OUT} \leq 60V$, PWM Dimming, TSSOP-38 |
| LT8705 | 80V $V_{IN}$ and $V_{OUT}$ Synchronous 4-Switch Buck-Boost DC/DC Controller | $2.8V \leq V_{IN} \leq 80V$, $1.3V \leq V_{OUT} \leq 80V$, Regulates $V_{OUT}$, $I_{OUT}$, $V_{IN}$, $I_{IN}$, 5mm × 7mm QFN-38, Modified TSSOP Package for High Voltage |
| LTC3789 | High Efficiency Synchronous 4-Switch Buck-Boost Controller | $4V \leq V_{IN} \leq 38V$, $0.8V \leq V_{OUT} \leq 38V$, 4mm × 5mm QFN-28, SSOP-28 |
| LTC3780 | High Efficiency Synchronous 4-Switch Buck-Boost Controller | $4V \leq V_{IN} \leq 36V$, $0.8V \leq V_{OUT} \leq 30V$, 5mm × 5mm QFN-32, SSOP-24 |
| LT3741/LT3741-1 | High Power, Constant Current, Constant Voltage, Step-Down Controller | $6V \leq V_{IN} \leq 36V$, 4mm × 4mm QFN-20, TSSOP-20 |
| LT3763 | 60V High Current Step-Down LED Driver Controller | $6V \leq V_{IN} \leq 60V$, 4mm × 4mm QFN-20, TSSOP-20 |
| LT3757/LT3757A | Boost, Flyback, SEPIC and Inverting Controller | $2.9V \leq V_{IN} \leq 40V$, Positive or Negative $V_{OUT}$, 3mm × 3mm DFN-10, MSOP-10 |
| LT3758 | High Input Voltage, Boost, Flyback, SEPIC and Inverting Controller | $5.5V \leq V_{IN} \leq 100V$, Positive or Negative $V_{OUT}$, 3mm × 3mm DFN-10, MSOP-10 |
| LT8490 | High Voltage, High Current Buck-Boost Battery Charge Controller with Maximum Power Point Tracking (MPPT) | $6V \leq V_{IN} \leq 80V$, $1.3V \leq V_{BAT} \leq 80V$, Automatic MPPT, 7mm × 11mm QFN-64 |
| LT8710 | Synchronous SEPIC/Inverting/Boost Controller with Output Current Control | $4.5V \leq V_{IN} \leq 80V$, Rail-to-Rail Output Current Monitor and Control, TSSOP-28E Package |

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